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High Performance and PVT Variation Tolerant Design for a Ternary Multiplier Using GNRFET Technology

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Abstract

The advent of the graphene nanoribbon field effect transistor (GNRFET) facilitates the design of digital circuits based on multi-valued logic. This is attributed to the transistor's capability to adjust the threshold voltage by modifying width of graphene nanoribbon. This paper aims to design and evaluate new 1-trit and 2-trit multiplier cells using ternary logic and 32-nm GNRFETs. The suggested designs' efficiency is compared with the recently published circuits at the presence of process-voltage-temperature (PVT) variations. The results obtained from HSPICE simulations demonstrate that our 1-trit ternary multiplier exhibits an 11.92% and 22.64% reduction in delay compared to Abbasian's and Rohani's designs, respectively. Furthermore, it achieves a decrease in power consumption (energy consumption) of at least 20.39% (46.25%), compared to the best design, that is Abbasian's design. Additionally, it requires the use of one less transistor compared to the most favorable design explored. Moreover, it demonstrates greater reliability against PVT variations. Nonetheless, when compared to Sudhakar's and Wang's designs, the suggested circuit exhibits a

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delay increase of 1.1 and 1.57 times, respectively. On the other hand, the proposed 2-trit ternary multiplier offers a power (energy) improvement of at least 6.86% (16.67%), compared to the top-performance design.

Keywords MVL · Multiplier · GNRFET · PDP · PVT

1 Introduction

Recently, the MVL circuits have earned a significant attention in digital logic systems. The MVL logics offer several advantages such as reduced chip area, lower interconnects, lower computation digits, low power and so on over the conventional binary logics [10, 12, 16, 28, 45]. The conventional binary logic utilizes only two logics i.e., logic '0' and '1' for digital computation [33]. The ternary is one type of MVL logic that utilizes three logics i.e., logic '0', '1' and '2', respectively [4–6, 15]. The design of ternary based digital circuits utilizing the traditional metal–oxide–semiconductor transistor (MOSFETs) demands for body biasing [11, 19, 20]. However, biasing the bulk terminals to MOSFETs increases the circuit complexity. In addition, scaling the channel length of the MOSFET in nanometer ranges experiences many issues such as consuming large power, high leakage currents and complex interconnects which degrades the entire performance of integrated circuit (IC) [6]. Thus, it is required to the design ternary logic schematics using alternate technologies like quantum dot FETs [17], reversible logic gates [27], single-electron FETs [13], carbon nanotube FETs (CNTFETs) [18, 29, 31, 44] and GNRFETs [1, 6, 15, 45]. Out of these technologies, the GNRFET is better technology to develop ternary schematics as it provides large mean-free-path (MFP), large mobility and ballistic transport [1, 6, 15, 45].

The GNRFET properties are compared to the advanced existing CNTFET technology in [6]. The GNRFET shows better properties over the CNTFET. In addition, GNRFETs also shows improved performance over the CNTFETs because the graphene nanoribbon (GNR) channel has smooth edges and lower number of defects [6]. Hence, due these advantages, GNRFETs are considered as best alternative to the CNTFETs.

Using GNRFETs various digital logic circuits are designed in [1, 3, 6, 7, 9, 15, 21, 24–26, 45]. The binary logic circuit designs are discussed in [3, 9, 21], ternary logic circuit designs are developed in [1, 6, 15, 45], quaternary schematics are described in [7, 25] and penternary logic designs are described in [24, 26]. The various digital logic schematics using GNRFET in traditional binary logics are developed in [3, 9, 21] to investigate the transient waveforms, voltage transfer characteristics (VTC) curves and various performance parameter. In [1, 6, 7, 15, 24–26, 45], the basic logic and complex arithmetic schematics are designed in ternary, quaternary and quinary logics. However, the quaternary and quinary logic have noise margins very low and issues of crosstalk are high. Whereas, in ternary, the noise margins higher and effect of crosstalk is tolerable.

The main focus of this work is to develop ternary multiplier using GNRFETs. Using GNRFETs, lot of works are presented on ternary multiplier (TMUL) circuits [1, 30, 39, 43]. The authors in [1, 30, 39, 43] developed the multiplier circuits using the GNRFET technology. These designs furnish unary functions and dual power supply

method to ternary circuits such as decoders or encoders or multiplexers. Moreover, these ternary multiplier circuits showed the performance improvements than the CNTFET ternary multiplier circuits. In [30], GNRFET based ternary multiplier circuit is designed using the 26 transistors and also compared with the existing multiplier circuits. This multiplier [30] shows reduced power and PDP on an average up to 37.30% and 22.22%, respectively, compared to the most superior investigated multiplier circuits. Furthermore, the authors of [30] are also compared their multiplier with the multiplier designed by the CNTFETs. The GNRFET multiplier shows enhanced power and PDP up to 41.77% and 30%, correspondingly and increased delay up to 25% compared to the CNTFET multiplier circuit [30]. A new design of ternary multiplier circuit is presented in [43]. The unary operators are utilized to degrade the transistors number and increase multiplier performance. According to simulations done in [43], the ternary multiplier (TMUL) design exhibits significant improvements in power by 71.18–76.36% and energy consumption by 67.78–86.54% compared to existing state-of-the-art TMUL designs. The GNRFETs and CNTFETs are used to design an extremely effective TMUL in [1]. The GNRFET TMUL reduces the power and energy up to 63.55% and 86.50%, respectively. Furthermore, utilizing GNRFET for designing TMUL increase delay by 1.32 × while reducing power and energy up to 56.07% and 42.92% over the CNTFET [1]. An efficient ternary multiplier circuit using GNRFET is presented in [39]. The proposed design achieved a minimum of 36.72% advancement in power and 28.17% improvement in energy efficiency over the existing multipliers. The multi-trit multipliers designs are presented in [35, 37, 41]. In [35], the authors proposed a multi-digit multiplier design based on capacitive logic and minority function. The design utilizes improved varieties of adders and multipliers to achieve high performance and energy efficiency. The multi-digit multiplier is based on the classical Wallace multiplier, which is high-speed multiplier architecture. The Wallace multiplier consists of several stages of partial product generation, reduction, and addition. The 3-trit multiplier is designed with adders and multipliers that show 16 times decrease in power and energy consumptions compared to conventional multiplier [35]. A low CNTFET-count multi-ternary multiplier is presented in [37]. Two custom full-adder configurations are also developed. Extensive HSPICE simulations reveal excellent performance with respect to power, delay as well as noise margin. A 3-trit Wallace tree CNTFET based multiplier utilizing 4-input adder, full and half adders are discussed [41]. The adders and multipliers utilizing 3:1 multiplexer that improves energy effectiveness within the design of multiplier. This multiplexer, leverage higher and standard threshold FETs, highly optimizes the multiplier power and computational speed. Furthermore, the proposed design degraded power consumption by minimizing the number of transitions in the signal generation schematics of both the multiplexer and arithmetic modules. The results demonstrate that 3-trit multiplier attained a 40% reduction in power consumption and a 51% improvement in PDP compared to the best designs reported in the literature [41]. Even though there are lot works on ternary multiplier circuits, in this study, we proposed a novel method to develop the GNRFET based ternary multiplier with reduced transistor count and high performance. The main efforts of the work are four folded namely:

- A novel method is presented to design the ternary multiplier schematic using GNRFETs.
- The simulation results on bandgaps and threshold voltages of GNRFET are presented for different GNR dimer lines.
- The various performance for the proposed TMUL circuit such as transistor count, delay, power, and PDP are also noted.
- Furthermore, a comparative analysis is also carried out for proposed TMUL circuit with the existing TMUL circuits to show effectiveness of proposed design technique.

The remainder of the paper is organized as follows: Sect. 2 discussed about ternary logic and their circuits. The discuss on GNRFET and its compatibility with the ternary logic is presented in Sect. 3. Section 4 discuss the proposed ternary multipliers and their operations. Section 5 describes the results and discussions, PVT variations and Monte Carlo simulations of the proposed multiplier. At last, conclusions are presented in Section 6.

2 Ternary Logic based System

In general, the digital logic system can be designed using the conventional logics i.e., binary logic. The binary logic consists of two logics '0' and '1'. The binary logic can be extended to the MVL which contains discrete logic states (D_{ll}) greater than 2. The various levels of logic can be characterized by the voltage or current or charge variables. The set of logics in MVL design can be characterized either as balanced or unbalanced modes. However, the binary logic is constrained to only unbalanced mode.

The ternary is one type of MVL, in which the D_{ll} value is 3. The balanced mode of ternary logic is characterized as '0', '1', and '2'. The unbalanced mode of ternary designs is presented in this work with power supply as 0.9 V. Table 1 provides the logic states of unbalanced mode and their corresponding voltages.

$$\begin{aligned} Out_1 &= \overline{I}_n = \{2 - I_n\} \\ Out_2 &= \left\{ \begin{array}{l} 0, \ I_n = 2 \\ 2, \ I_n \neq 2 \end{array} \right\} \\ Out_3 &= \left\{ \begin{array}{l} 0, \ I_n \neq 0 \\ 2, \ I_n = 0 \end{array} \right\} \end{aligned} \tag{1}$$

Table 1 Unbalanced ternary logics and voltage levels

Logic states	Voltage (V)
0	0
1	$0.5V_{DD}$
2	V_{DD}

Table 2 Inverter truth table

Input (In)	STI (Out_1)	PTI (Out_2)	NTI (Out_3)
0	2	2	2
1	1	2	0
2	0	0	0

Depending on the functionality, the ternary logic consists three inverters like standard ternary inverter (STI), negative ternary inverter (NTI) and positive ternary inverter (PTI). The mathematical expressions of these inverters are provided in Eq. (1), where I_n is input and Out_1, Out_2 and Out_3 are outputs [6, 45]. The inverters truth tables are illustrated in Table 2.

3 GNRFET and its Compatibility with the Ternary Logic

The traditional MOSFET suffers with the short-channel effect, gate-leakage current, consuming large power and losing its reliability due to reduce its channel in to nanometers. These problems have forced the research scientists to find the alternate material over the MOSFET that has capability to scale down in to nanometers. Out of many materials, GNR is conceived as the best material to replace as channel because of its wonderful electronic, thermal and mechanical properties [6]. The GNR is sheet of carbon atoms produced from the graphene material. The GNRs are classified as two types (1) arm-chair and (2) zig-zag GNRs, respectively. The structures of these GNRs are shown in Fig. 1. The zig-zag GNRs always acts a metal and they cannot used as channel. Where, the arm-chair GNR acts either as metal or semiconductor depending on dimer line (D_{ac}). The arm-chair GNRs which act as semiconductors can be used as channel materials. The arm-chair GNRs act as metal for $D_{ac} = 3\,l + 2$ and it act as semiconductor for $D_{ac} = 3\,l$ or $D_{ac} = 3\,l + 1$ where l is an integer [6].

The GNR is placed in substrate to fabricate the GNRFET. Similar to the MOSFET, the GNRFET also have gate, body, source and drain as its regions. Here also the gate region decides the ON and OFF states of the GNRFET. In GNRFET, the channel portion has the intrinsic type GNRs, whereas the drain and source terminals are highly doped with acceptors or donors [6, 15]. Figure 2 illustrates GNRFET structure.

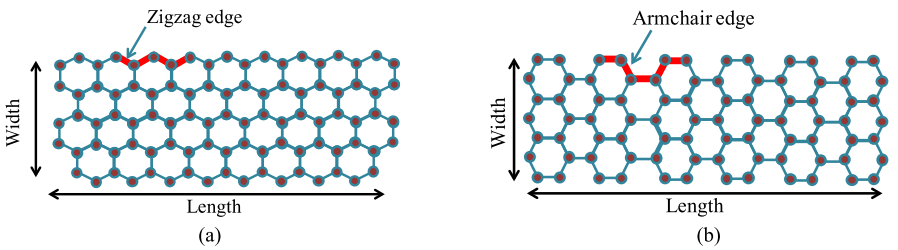
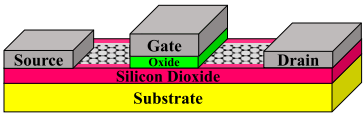


Fig. 1 Structure of GNR (**a**) Zig-zag GNR and (**b**) Arm-chair GNR

Fig. 2 Structure of GNRFET



The GNRFET threshold-voltage (V_{GS}), band gap (B_{GS}) and GNR width (W_{GS}) are calculated from the Eqs. (2)–(5), respectively. The parameters used in these equations are discussed in Table 3. Using these equations, the B_{GS} and V_{GS} values are calculated and evaluated with Quantum ATK tool. Figure 3 shows that B_{GS} and V_{GS} values for various dimer lines. It observed that the calculated values and values obtained from the ATK simulator are similar. Moreover, I-V characteristic of GNRFETs are investigated for different dimer lines and shown in Fig. 4. The GNRFET I-V characteristics looks similar to traditional MOSFETs. Hence, because of possibility of different threshold voltages and similar I-V structures of MOSFET, GNRFET technology can be used to implement with ternary designs. The circuit model of GNRFET shown in Fig. 5 is used in this work. The GNRFET charge (Q_{ch}) is stated in Eq. (6). The exhaustive discussion on $C_{G,S}$, $C_{G,D}$ and parameters utilized in Eq. (6) is described in [22, 23].

$$V_{GS} = {}^{B_{GS}}/_{3e_C} \tag{2}$$

Table 3 The various parameters and description used in Eqs. (3)-(6)

Parameter	Description	Value
e_C	Charge of Electron	$1.60217663 \times 10^{-19}$C
D_{ac}	Dimer Line	$\beta = 0.066$ for $3\,l + 2$, $\beta = 0.4$ for $3\,l + 1$, $\beta = 0.27$ for $3\,l$
h_p	Plank's Constant	6.5×10^{-16} eV·s
V_{fr}	Fermi Velocity	1×10^6 m/s
a	Carbon–Carbon Distance	0.142 nm

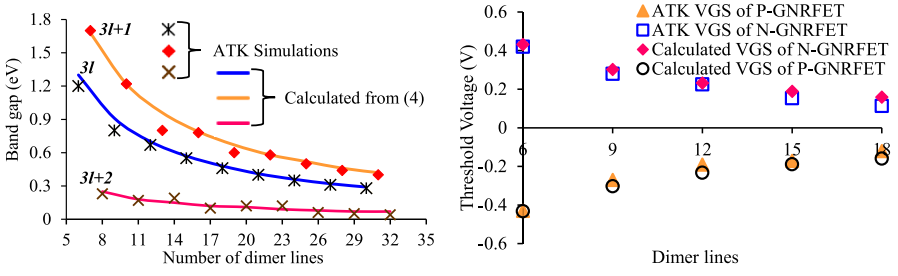


Fig. 3 Calculated and ATK values of (**a**) Band Gap and (**b**) Threshold Voltage

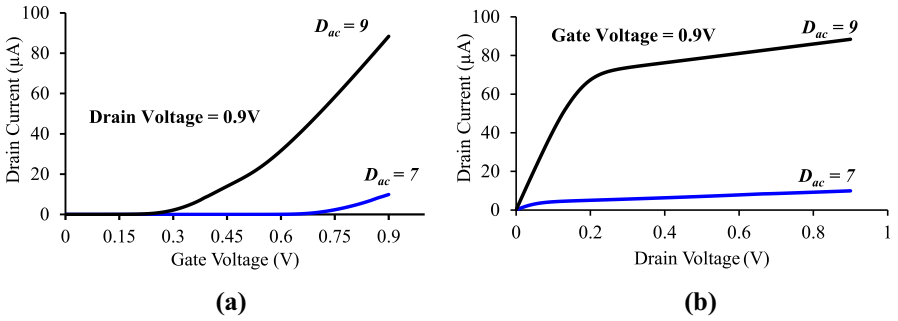


Fig. 4 Characteristics of GNRFET (**a**) I_{DS} Vs V_{GS} and (**b**) I_{DS} Vs V_{DS}

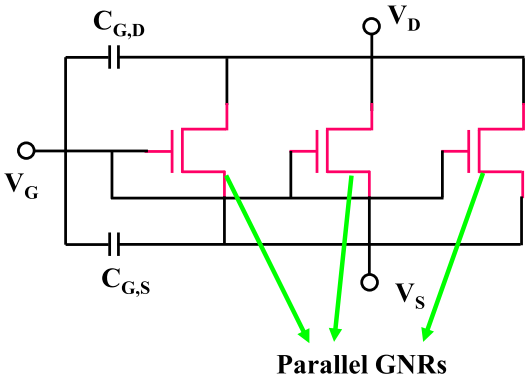


Fig. 5 SPICE Circuit model of GNRFET

$$B_{GS} = 2|\beta|\nabla E \tag{3}$$

$$\nabla E = {}^{h_p V_{fr} \pi}/_{W_{GS}} \tag{4}$$

$$W_{GS} = \left(\frac{1 + D_{ac}}{2}\right)\sqrt{3}a \tag{5}$$

$$\begin{aligned} Q_{ch} = & \frac{qL_{ch}}{2} \sum_{\alpha} [-n_\alpha(q\Psi_{ch} - \varepsilon_\alpha - qV_s) \\ & - n_\alpha(q\Psi ch - \varepsilon_\alpha - qV_D) + T_r(\Psi_{ch,D}) \\ & \cdot p_\alpha(qV_D - q\Psi_{ch} - \varepsilon_\alpha)] \end{aligned} \tag{6}$$

4 Proposed GNRFET-based Ternary Multiplier Circuits

4.1 Proposed Single-Trit Ternary Multiplier

Firstly, the main unary operators (i.e., NTI and PTI circuits), decisive literal A_1, and positive ternary two-input NAND gate circuit using GNRFET devices are designed. Then, these three circuits are employed in the proposed TMUL circuit design. Figure 6a and b show the schematics of GNRFET-based NTI and PTI, where A is ternary input digit, while A_N and A_P are the resulting ternary output digits.

As shown in Fig. 6c, when A is '0', T3 is turned on by A_N = '2', which pulls down A_1 to ground and when A is '1' or '2', transmission gate (T1 and T3) is turned on and connects A_1 with A_P. The complement of A_1 is generated by a binary inverter (T4 and T5).

The standard ternary two-input NAND (ST-NAND2) gate is a one of the operators in ternary circuits, which is defined in Eq. (7), where A and B are two ternary input digits. The functionality of ST-NAND2 gate is given in Table 4. As observed in Table 4, when at least one of the inputs is '0', *output* becomes '2', when one input is '1' and other one is '2', *output* becomes '1', and finally, when both inputs are '2', *output* becomes '0'.

$$\mathrm{ST-NAND2} = \overline{A \cdot B} = \overline{\min(\mathrm{A},\ \mathrm{B})} \tag{7}$$

Positive ternary NAND (PT-NAND2) is an especial mode of ST-NAND2 gate, in which logical value '2' appears in the output instead of '1'. Table 4 also gives functionality of PT-NAND2 gate and contains the unary operator B_P, which helps us during the design. Figure 7a and b respectively show schematic and output of proposed GNRFET PT-NAND2 gate. As depicted in Fig. 7a, two ternary inputs are categorized as A and B, while ternary output is categorized as A_2B_2.

The function of presented GNRFET-based PT-NAND2 gate is as follows.

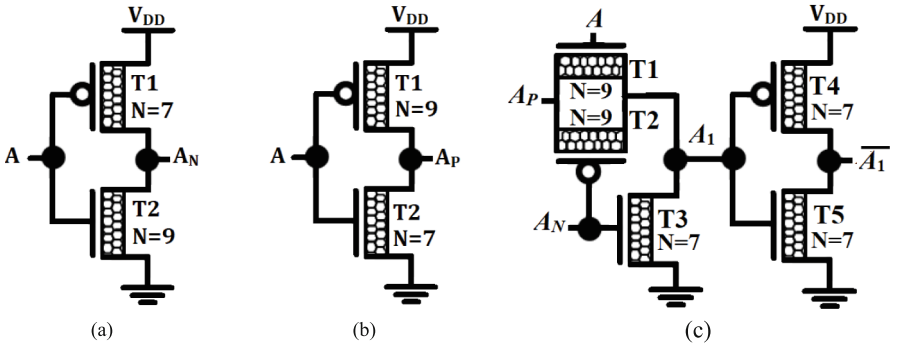


Fig. 6 Schematic diagrams of the GNRFET-based (**a**) NTI, **b** PTI [41], and **c** decisive literal A_1 and its complement

Table 4 Functionality table of the PT-NAND2 gate, with incorporated unary operator B_P

Inputs		Unary operator	ST-NAND2	PT-NAND2
A	*B*	B_P	*Out*	*Out*
0	0	2	2	2
0	1	2	2	2
0	2	0	2	2
1	0	2	2	2
1	1	2	1	2
1	2	0	1	2
2	0	2	2	2
2	1	2	1	2
2	2	0	0	0

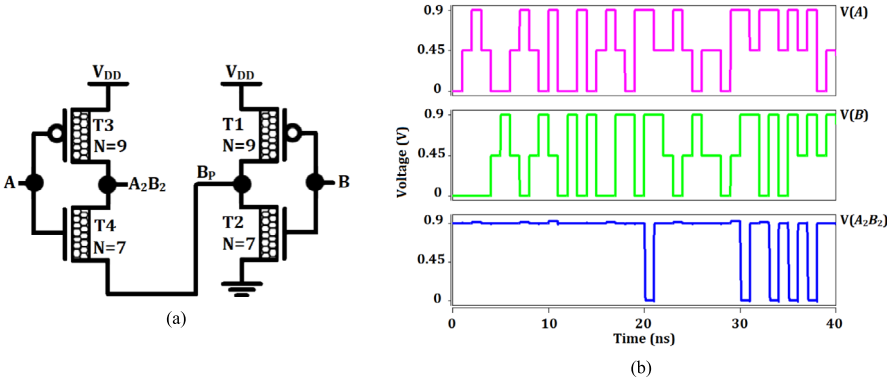


Fig. 7 Proposed GNRFET-based PT-NAND2 gate. **a** Schematic diagram and **b** Transient response

- When A is equal to '0', A_2B_2 becomes '2' through turned-on T3. In this situation, the input value of B is does not care.
- When A becomes '1', the status of T3 will not change. Then, A_2B_2 will be remained at logic '2'. In this situation, the input value of B is does not care.
- When A becomes equal to '2', T4 is turned on. If B is either equal to '0' or '1', T1 is turned on and make B_P high ('2'). Then, A_2B_2 becomes equal to B_P ('2') through turned-on T4. If B is '2', T2 is turned on and make B_P low ('0'). Then, A_2B_2 becomes equal to B_P ('0') through turned-on T4 transistor.

Next, the proposed TMUL schematic is designed. Table 5 presents the operational table for TMUL circuit. In this table, A and B represent two ternary input digits, while *Product* and *Carry* denote the resulting ternary output digits. We have also included unary operators (A_N, A_P, B_N, and B_P) and the output of PT-NAND2 gate (A_2B_2) within Table 5. The purpose of this inclusion is to facilitate a more thorough understanding of the circuit's behavior and aid in its design process. Figure 8 depicts the schematic

Table 5 Functionality table of the TMUL circuit, with incorporated unary operators and PT-NAND2 gate's output

Inputs		Unary operators				PT-NAND2	Outputs	
A	B	A_N	A_P	B_N	B_P	A_2B_2	Product	Carry
0	0	2	2	2	2	2	0	0
0	1	2	2	0	2	2	0	0
0	2	2	2	0	0	2	0	0
1	0	0	2	2	2	2	0	0
1	1	0	2	0	2	2	1	0
1	2	0	2	0	0	2	2	0
2	0	0	0	2	2	2	0	0
2	1	0	0	0	2	2	2	0
2	2	0	0	0	0	0	1	1

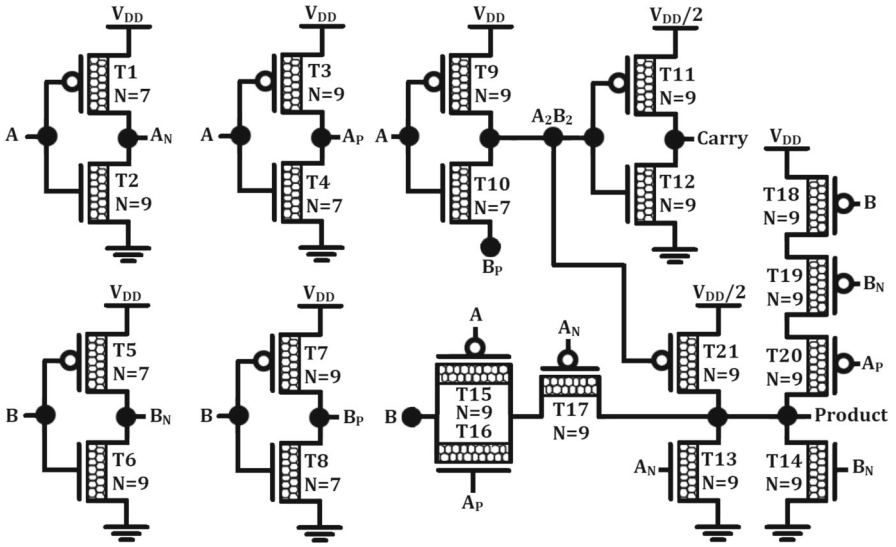


Fig. 8 Schematic diagram of proposed TMUL circuit, implemented with 21 transistors

of proposed GNRFET-based TMUL circuit.

The circuit generation for *Product* output can be designed as follows:

- When *A* is '0' and *B* is either '1' or '2', *Product* becomes '0' through turned-on T13.
- When *B* is '0' and *A* is either '1' or '2', *Product* becomes '0' through turned-on T14.
- When both inputs are '0', *Product* becomes '0' through turned-on T13 and T14.

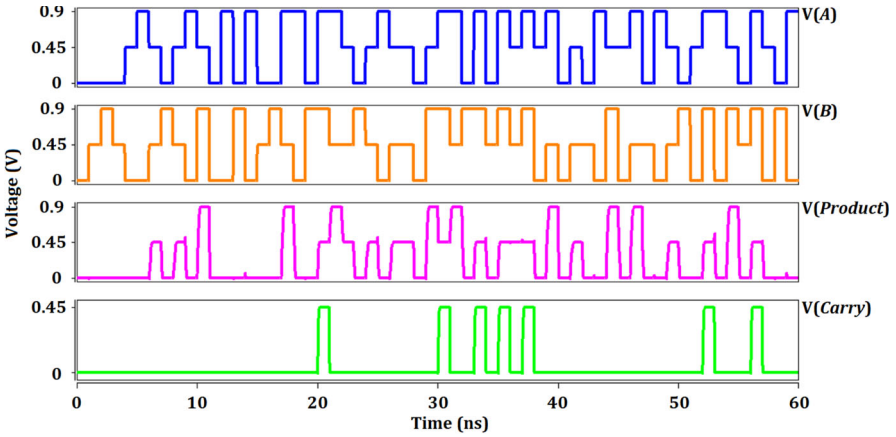


Fig. 9 Transient responses of proposed TMUL circuit

- When *A* is '1', *Product* is equal to *B*. In this situation, *B* is transferred to *Product* output through turned-on T15, T16, and T17.
- When *A* is '2' and *B* is '1', *Product* becomes '2' through turned-on T18, T19, and T20.
- When both inputs are '2', *Product* becomes '1' through turned-on T21.

The circuit generation for *Carry* output can be designed as follows:

- When *A* is '0' and *B* is either '1' or '2', *Carry* becomes '0' through turned-on T12.
- When *B* is '0' and *A* is either '1' or '2', *Carry* becomes '0' through turned-on T12.
- When both inputs are '2', *Carry* becomes '1' through turned-on T11.

Figure 9 illustrates output of proposed GNRFET TMUL circuit and it is obvious that the proposed circuit operates well.

4.2 Proposed Two-Trit Ternary Multiplier

To measure the feasibility of single-trit TMUL within larger computational circuits, a two-trit TMUL is developed on established Wallace tree multiplier [42]. Figure 10 illustrates the block diagram of this 2-trit TMUL. As evident from the diagram, the implementation necessitates four single-trit TMUL circuits, two ternary full adder (TFA) circuits, and one ternary half adder (THA) circuit. Notably, THA block requires solely a *Sum* circuit due to its input values (c_1 and c_2) being restricted to the range of '0' and '1'.

The THA circuit, as defined by the truth table in Table 6, accepts two ternary inputs, *A* and *B*, and produces two outputs, including *Sum* and *Carry*. These outputs represent the sum and carry digits resulting from the addition of the two ternary inputs. This circuit can be readily implemented and designed using Eq. (8), which provides a concise mathematical representation of its logic. Figure 11 presents the transistor-level schematic diagram of the proposed GNRFET-based THA circuit, accompanied

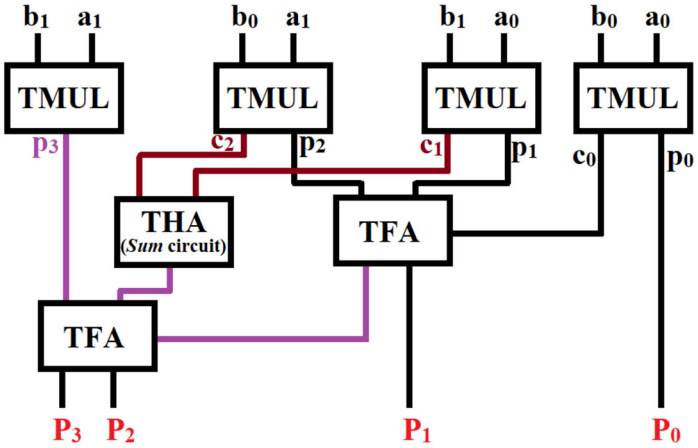


Fig. 10 A block diagram depicting the architecture of the two-trit TMUL circuit based on Wallace tree multiplier [36]

Table 6 The truth table of the THA circuit

A/B	B (0)	B (1)	B (2)
Sum			
A (0)	0	1	2
A (1)	1	2	0
A (2)	2	0	1
Carry			
A (0)	0	0	0
A (1)	0	0	1
A (2)	0	1	1

by its transient response. This diagram offers a detailed visualization of the circuit's physical realization, while the transient response provides insight into its dynamic behavior over time.

$$\begin{aligned} Sum &= A.B_0 + (1.A_0 + 2.A_1 + 0.A_2).B_1 + (2.A_0 + 0.A_1 + 1.A_2).B_2 \\ Carry &= 0.B_0 + (0.A_0 + 0.A_1 + 1.A_2).B_1 + (0.A_0 + 1.A_1 + 1.A_2).B_2. \end{aligned} \tag{8}$$

The TFA circuit, a fundamental component of ternary logic systems, performs addition operations on two ternary inputs (A and B) and a carry-in input (C), generating two ternary outputs, including the *Sum* and the *Carry* (carry-out). The proposed TFA circuit design employing GNRFETs is depicted in Fig. 12. The proposed design is based on the proposed THA circuit, leveraging the unique electrical properties of GNRFETs to realize the necessary ternary logic operations.

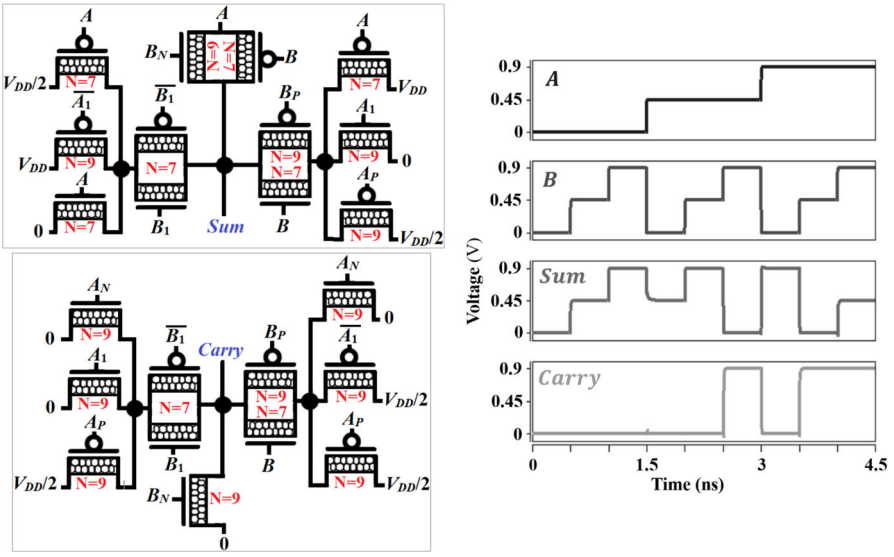


Fig. 11 GNRFET THA, along with transient response

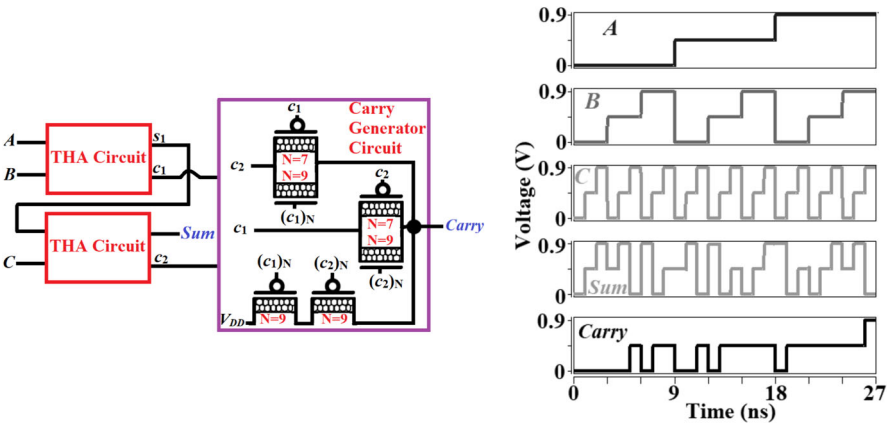


Fig. 12 Proposed GNRFET-based TFA circuit, along with transient response

As illustrated in Fig. 12, the upper THA block performs addition on the two primary inputs A and B, producing an intermediate *Sum* (s_1) and a first carry (c_1). Subsequently, the lower THA block sums the intermediate *Sum* (s_1) with the carry-in input (C), yielding the final *Sum* output of the TFA circuit and a second carry (c_2). Since both c_1 and c_2 range from '0' to '1', the final *Carry* output of the TFA is generated by employing two transmission gates and two serially connected p-type GNRFETs.

By integrating the designs of single-trit TMUL, THA, and TFA circuits into the 2-trit TMUL block diagram depicted in Fig. 10, we are able to perform multiplication

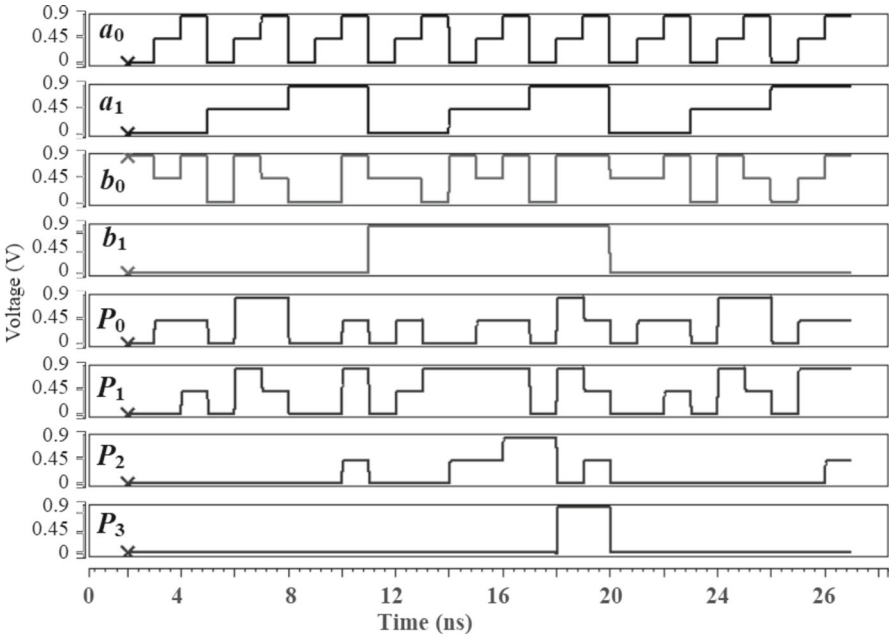


Fig. 13 The transient response of the 2-trit TMUL circuit

operations on two-trit ternary inputs $A = a_1a_0$ and $B = b_1b_0$, resulting in the outputs ($P = P_3P_2P_1P_0$). Figure 13 confirms the functional correctness of the implemented 2-trit TMUL.

5 Results and Discussions

5.1 Simulation Setup

The proposed TMUL circuits are simulated using Synopsis HSPICE software and GNRFET technology with 32 nm GNR length [2, 8, 40]. Of the various genres of GNRFETs, MOS-like GNRFET devices are better suited for the design and simulation of proposed schematic because of their provision of high on-to-off currents ratio (I_{ON}/I_{OFF}) [1]. Table 7 provides a listing of SPICE parameters pertaining to the GNRFET utilized in the simulation.

Table 8 presents our simulation results for I_{OFF}, I_{ON}, the I_{ON}/I_{OFF} ratio, and threshold voltage (V_{th}) of n-type MOS-GNRFET device with the parameters provided in Table 7. We have taken special conditions into account to simulate proposed TMUL schematic, as well as other TMUL schematics that have been reviewed and are available in the literature [1, 30, 39, 43]. The specifications encompass a supply voltage (V_{DD}) = 0.9Volts, temperature = 300˚K, input-swing = 20pS, frequency = 1 GHz, and four-triple fan outputs (FO4) serving as output loads. The STI introduced in [39] is

Table 7 Physical of GNRFET

Parameters	Descriptions	Values
V_{DD}	Supply (V)	0.9
$Temp$	Temperature (˚K)	300
L_{CH}	Channel length (nm)	32
T_{ox}	Oxide thickness (nm)	1.5
$2W_{sp}$	Distance between two adjacent GNRs (nm)	2
N_{GNR}	GNRs numbers	6
H_{ox}	Gate constant dielectric	4
f_{dop}	Doping-fraction	0.001
P_r	Line edge roughness (%)	0

Table 8 I_{ON}, I_{OFF}, I_{ON}/I_{OFF} and V_{th} of n-type MOS-GNRFET w.r.t N

Parameter	N= 7	N= 9	N= 10
I_{ON} (μA)	17.8	136.34	77.52
I_{OFF} (A)	1.1 f	0.26 n	0.42 p
I_{ON}/I_{OFF}	1.62×10^{10}	5.24×10^{5}	1.85×10^{8}
V_{th} (V)	0.6	0.24	0.4

utilized for the purpose of generating FO4. To guarantee an equitable comparison, all TMUL circuits based on MOS-GNRFET re-simulated utilizing simulation test-bench and GNRFET parameters outlined in Table 7.

5.2 Transient Responses of GNRFET-TMUL

Figures 9, 13 illustrated output responses of proposed TMUL circuits operating under specified conditions (FO4, $V_{DD} = 0.9$ V, T = 300 ˚K, F = 1 GHz). The input waveform depicted encompasses all-distinct combinations with corresponding outputs being readily discernible.

5.3 Result Analysis of Single-trit TMUL

5.3.1 FET Count and Total-Width Comparisons

The comparisons among proposed and studied single-trit TMUL designs [1, 30, 39, 43] is presented in Table 9. The findings indicate a notable decrease in no of FETs when compared to designs of [1, 30, 39, 43]. Additionally, the total width, evaluated by adding the width of all FETs [30], demonstrates a decrease in area when compared to the comparison TMUL designs [1, 30, 39, 43].

Table 9 Comparisons of schematic characteristics between proposed single-trit TMUL with the existing single-trit TMUL circuits

1-trit TMUL	Transistor count	Total width (nm)	Dual-VDD technique	No. of dimer lines
Abbasian [1]	22	385.032	Yes	2
Rohani [30]	23	401.46	Yes	2
Sudhakar [39]	26	404.412	Yes	2
Wang [43]	26	450.744	Yes	2
Proposed TMUL	21	368.604	Yes	2

Table 10 Performance comparisons of proposed single-trit TMUL design with the existing single-trit TMUL circuits for normal conditions

1-trit TMUL	Delay (ps)	Power (μW)	PDP (aJ)
Abbasian [1]	26	0.152	5.57
Rohani [30]	29.6	0.237	6.11
Sudhakar [39]	20.9	0.386	5.06
Wang [43]	14.6	0.399	5.83
Proposed TMUL	22.9	0.121	2.72

5.3.2 Normal Conditions

Table 10 presents maximum delay, power consumption, and energy efficiency of proposed and investigated single-trit TMUL designs [1, 30, 39, 43]. The comparisons were conducted under identical conditions ($V_{DD} = 0.9$ V, T = 300 ˚K, F = 1 GHz, and FO4). The below explanation afforded for these results:

- In comparison to the Abbasian's design [1], there has been a notable 11.92% enhancement in delay, a substantial 20.08% enhancement in power, and a remarkable 51.27% enhancement in energy.
- In comparison to the Rohani's design [30], there has been an improvement of 22.68% in delay, 48.65% in power, and 55.57% in energy.
- In comparison to Wang's design [43], our findings indicate a 56.85% escalation in delay, a 69.47% enhancement in power, and a 53.39% advancement in energy.
- In comparison to the Sudhakar's design [39], there has been a 9.57% increase in delay, a 68.43% enhancement in power, and a 46.34% improvement in energy.

5.3.3 Study of *VDD* Variation

The Fig. 14 and Table 11 presents the comparisons of the delay, power and energy of proposed and other single-trit TMUL circuits under the conditions of T = 300 ˚K, F = 1 GHz, and FO4. Based on the findings presented in the table, it is evident that higher voltage leads to increased power and reduced delay due to enhanced carrier

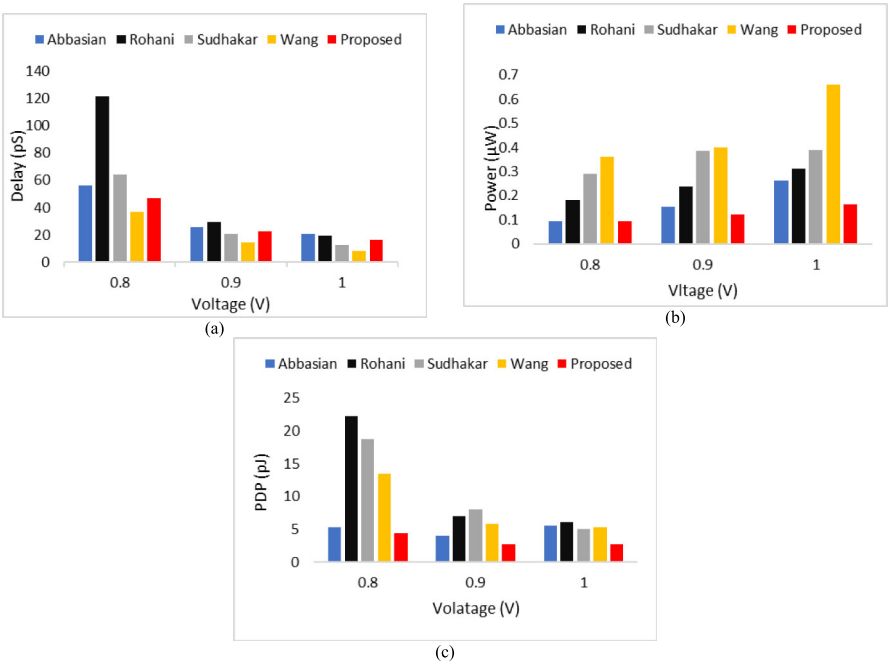


Fig. 14 Impact of V_{DD} variations on the performance of investigated single-trit TMUL circuits. **a** delay, **b** power, and **c** PDP

mobility. In comparison to alternative designs, the proposed approach demonstrates lower power consumption and energy usage.

5.3.4 Study of Temperature Variation

The Fig. 15 and Table 12 illustrates comparisons of delay, power and energy of proposed single-trit TMUL alongside those of other single-trit TMUL in a scenario where $V_{DD} = 0.9$ V, F = 1 GHz, and FO4. Depending on the result presented in the table and the subsequent analysis, it is evident that an increment in temperature results in enhanced carrier mobility and speed, leading to higher power and reduced delay. Compared to alternative designs, the proposed approach exhibits lower power usage and energy consumption.

5.3.5 Study of Output Load Variation

The impact of output load variations on performance of analyzed single-trit TMUL designs, including the circuits that were suggested, is studied in Fig. 16 and Table 13 with regard to delay, power, and energy. The experiments were carried at a $V_{DD} = 0.9$ V, T = 300 ˚K, F = 1 GHz, and with different output load values. As anticipated, higher output loads resulted in increased latency, power, and energy across all circuits.

Table 11 Performance comparisons of proposed single-trit TMUL design and other single-trit TMUL designs for different V_{DD}

1-trit TMUL	VDD = 0.8 V			VDD = 0.9 V			VDD = 1 V		
	Delay (pS)	Power (μW)	PDP (aJ)	Delay (pS)	Power (μW)	PDP (aJ)	Delay (pS)	Power (μW)	PDP (aJ)
Abbasian [1]	56.2	0.094	5.30	26	0.152	3.96	21.1	0.264	5.57
Rohani [30]	121.5	0.183	22.26	29.6	0.237	7.02	19.6	0.312	6.11
Sudhakar [39]	64.5	0.290	18.73	20.9	0.386	8.06	13	0.389	5.06
Wang [43]	37	0.363	13.44	14.6	0.399	5.83	8.09	0.661	5.35
Proposed MUL	47	0.094	4.42	22.9	0.121	2.79	16.4	0.166	2.72

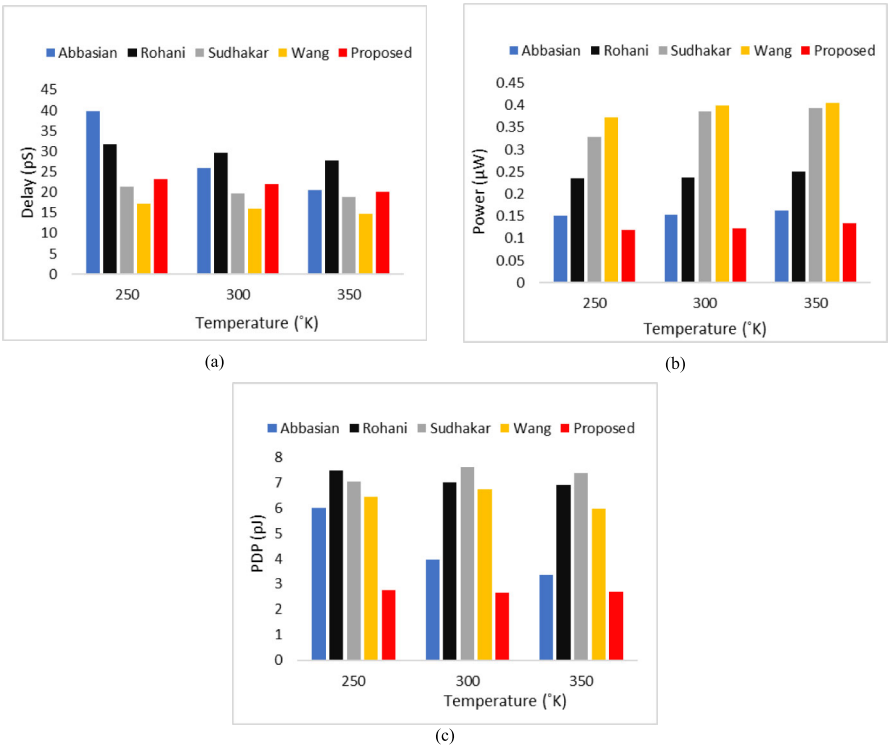


Fig. 15 Impact of temperature variations on performance of investigated single-trit TMUL circuits. **a** delay, **b** power, and **c** PDP

Out of all simulated output loads, TMUL circuit proposed exhibited minimal power and energy consumption compared to other designs that were proposed.

5.3.6 Monte Carlo Simulation

Monte-Carlo (MC) analysis is an approach used to investigate significant process changes and their impacts of the circuit performance. The number of MC simulation's samples conducted in this study is set to 30. If a circuit operates correctly for every 30 samples, the probability of its correct operation exceeds 80% when considering 99% of the possible values of the components [38]. MOS-GNRFET device parameters, such as channel length (L_{ch}), oxide thickness (T_{ox}), and channel width (W_{ch}), follow independent Gaussian distributions with variations of $\pm$ 10% or $\pm$ 3σ [1]. Tables 14, 15, 16, respectively show the MC analysis for the power, delay, and PDP of proposed and the comparison single-trit TMUL circuits [1, 30, 39, 43]. From these tables, it is noted that proposed TMUL circuit has more robustness against process variation because it shows lower standard variation.

Table 12 Performance comparisons of proposed single-trit TMUL design with existing single-trit TMUL designs for temperatures

1-trit TMUL	T = 250 K			T = 300 K			T = 350 K		
	Delay (pS)	Power (μW)	PDP (aJ)	Delay (pS)	Power (μW)	PDP (aJ)	Delay (ns)	Power (μW)	DP (aJ)
Abbasian [1]	39.8	0.151	6.02	26	0.152	3.96	20.5	0.164	3.35
Rohani [30]	31.8	0.235	7.47	29.6	0.237	7.02	27.7	0.250	6.91
Sudhakar [39]	21.4	0.329	7.05	19.7	0.386	7.60	18.8	0.393	7.39
Wang [43]	17.3	0.372	6.44	15.9	0.399	6.75	14.7	0.405	5.96
Proposed TMUL	23.3	0.119	2.77	21.9	0.122	2.67	20.1	0.134	2.69

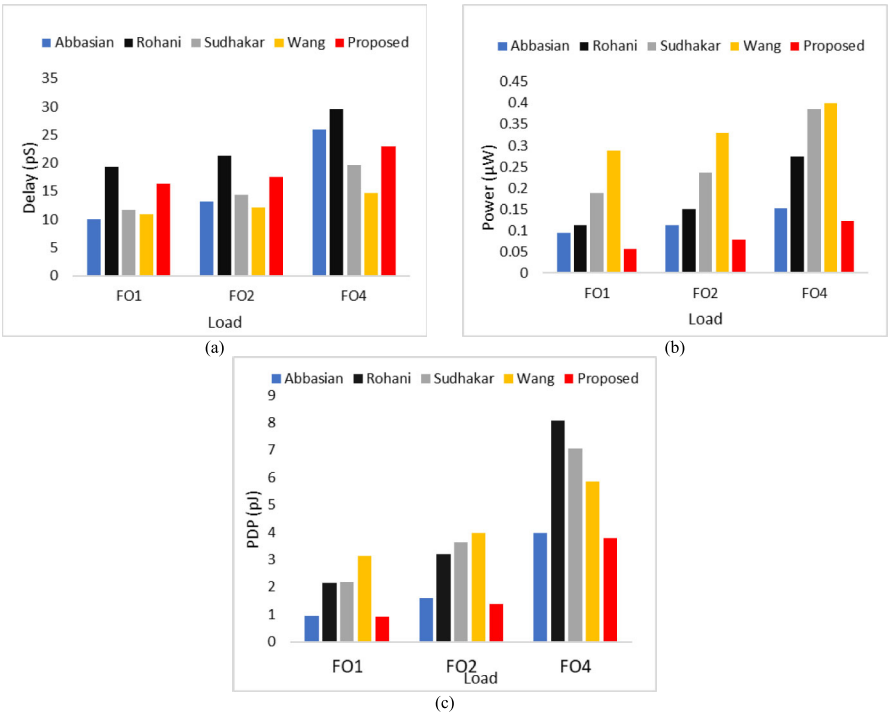


Fig. 16 Impact of output loads on performance of single-trit TMUL circuits. **a** delay, **b** power, and **c** PDP

5.4 Result Analysis of Two-trit TMUL

The delay, power, and PDP of proposed 2-trit TMUL circuit are compared to traditional 2-trit TMUL designs [14, 32, 34, 36] at $V_{DD} = 0.9$ V. The simulation outcomes are showed in Table 17. As evident from this table, the Sharma's design shows the worst performance, which can be explained as below:

- It uses 3:1 ternary multiplexer (TMUX) and self-shift operator circuit with serially connected transmission gates within the single-trit TMUL circuit, which degrade speed.
- It uses single shift operator b dual shift operator, which have series-connection transmission gates, resulting in speed reduction.
- A TFA circuit has been used, wherein 2:1 TMUXs and 3:1 TMUXs have been connected to each other in series, creating three stages, which degrade speed.
- A THA circuit has been used, wherein 2:1 TMUXs and 3:1 TMUXs have series-connection, creating two stages, which degrade the speed.
- The power consumption is increased owing to using lots of 2:1 TMUX and 3:1 TMUX circuits and capacitances.

The Shahrom's design [34] offers better performance metrics compared to the Sharma's design [36] but still cannot outperform proposed 2-trit TMUL circuit. This is due to following reasons:

Table 13 Performance comparison of proposed single-trit TMUL design with existing single-trit TMUL designs for various Output loads

1-trit TMUL	FO1			FO2			FO4		
	Delay (pS)	Power (μW)	PDP (aJ)	Delay (pS)	Power (μW)	PDP (aJ)	Delay (pS)	Power (μW)	PDP (aJ)
Abbasian [1]	10	0.094	0.94	13.12	0.113	1.58	26	0.152	3.96
Rohani [30]	19.3	0.111	2.15	21.3	0.150	3.20	29.6	0.273	8.09
Sudhakar [39]	11.6	0.189	2.19	14.3	0.236	3.63	19.7	0.386	7.07
Wang [43]	10.9	0.288	3.13	12.1	0.329	3.98	14.6	0.399	5.84
Proposed MUL	16.3	0.057	0.93	17.6	0.078	1.38	22.9	0.122	3.79

Table 14 Monte Carlo power simulation results for the proposed and various single-trit TMUL designs available in the literature

1-trit TMUL	Power analysis			
	Mean (μW)	Std. deviation (nW)	Max. Power (μW)	Min. Power (μW)
Abbasian [1]	0.1577	11.47	0.1769	0.1487
Rohani [30]	0.2376	0.589	0.2535	0.1974
Sudhakar [39]	0.1511	2.87	0.1741	0.1476
Wang [43]	0.2806	18.4	0.3245	0.2486
Proposed work	0.1216	0.228	0.1319	0.1113

Table 15 Monte Carlo Delay simulation results for the proposed and various single-trit TMUL designs available in the literature

1-trit TMUL	Delay analysis (pS)			
	Mean	Std. deviation	Max. Delay	Min. Delay
Abbasian [1]	33.03	0.615	38.91	25.32
Rohani [30]	29.64	0.251	30.01	26.37
Sudhakar [39]	27.55	0.246	32.92	24.51
Wang [43]	29.37	0.205	31.65	27.20
Proposed work	33.02	0.157	34.85	32.34

Table 16 Monte Carlo PDP simulation results for the proposed and various single-trit TMUL designs available in the literature

1-trit TMUL	PDP analysis (aJ)			
	Mean	Std. deviation	Max	Min
Abbasian [1]	5.208	0.324	5.712	4.872
Rohani [30]	7.043	0.066	7.139	6.959
Sudhakar [39]	4.163	0.083	4.254	4.032
Wang [43]	8.241	0.523	8.602	7.343
Proposed work	4.017	0.046	4.125	3.931

- It uses a THA circuit designed using 3:1 TMUXs and ternary decoder, which reduces speed and increases power usage.
- The THA is then used to design the TFA, which degrades speed of the TFA circuit.

Compared to Sharma's design [36], Sahoo's design [32] consumes less power while providing the lowest delay among the competing designs. However, the proposed 2-trit

Table 17 Performance comparisons of proposed 2-trit TMUL design with the existing 2-trit TMUL circuits for normal conditions

2-trit TMUL circuits	Delay (ns)	Power (μW)	PDP (aJ)
Sharma [36]	97.3	2.6	0.253
Shahrom [34]	72	1.3	0.094
Sahoo [32]	46.3	1.68	0.078
Sirugudi [14]	86.5	1.02	0.088
Proposed work	68.1	0.95	0.065

TMUL circuit still has lower PDP compared to Sahoo's design due to the following factors:

- Sahoo's design [32] omits the use of capacitances for summing the input logic, resulting in lower power consumption than Sharma's design [36]. However, the design experiences short-circuit phenomenon within its unary operators many times, which increases power consumption compared to other designs.
- The design's shortest critical path contributes to its superior delay performance.
- The incorporation of multiple unary operators and 3:1 TMUX circuits in Sahoo's design elevates power consumption.

Therefore, this unresolved issue continues to hinder the circuit's power efficiency and performance optimization. As a result, the circuit's potential for widespread adoption and practical applications remains constrained by its inherent power consumption concerns.

Sirugudi's proposed circuit [14] employs a combination of cascaded 2:1 TMUX circuits and dual-V_{DD} techniques. While these techniques aim to extend the critical path and reduce power dissipation, the design exhibits performance limitations in comparison to the proposed design. As observed from Table 17, Sirugudi's circuit demonstrates higher delay, power consumption, and PDP compared to the suggested design. These factors hinder its efficiency and suitability for practical applications.

The proposed 2-trit TMUL circuit improves delay by 30.01%, 5.42%, and 21.27% compared to Sharma's design [36], Shahrom's design [34], and Sirugudi [14], respectively. However, it incurs delay penalty of 1.47 times compared to Sahoo's design [44]. Alternatively, proposed design reduces power by 63.46%, 26.92%, 43.45%, 6.86%, and PDP by 74.31%, 30.85%, 16.67%, and 26.14% compared to Sharma's design [36], Shahrom's design [34], Sahoo's design [32], and Sirugudi [14], respectively.

6 Conclusion

The utilization of emerging graphene nanoribbon field effect transistor (GNRFET) devices in combination with ternary logic for the design of very large-scale integration (VLSI) designs overcomes the limitations associated with binary and CMOS transistors. This can be attributed to the GNRFET's capacity to control the threshold voltage values by changing width of GNR. This research paper capitalizes on this intriguing property to propose novel and efficient single-trit and multi-trit ternary

multiplier (TMUL) circuits. To evaluate the effectiveness of the suggested circuits, a comprehensive comparison was conducted against previously published ternary multiplier circuits, employing 32-nm channel GNRFET devices and the Synopsis HSPICE simulator, while considering process-voltage-temperature (PVT) variations. The results obtained from our simulations clearly demonstrate that the proposed single-trit TMUL design outperforms Abbasian's and Rohani's designs, showcasing a remarkable reduction in delay by 11.92% and 22.64%, respectively. Moreover, the proposed circuit achieves a significant decrease in power consumption and energy consumption, amounting to at least 20.39% and 46.25%, respectively. Another noteworthy advantage of our proposed circuit is its ability to employ one less transistor compared to the most favorable design explored. Furthermore, the proposed circuit exhibits enhanced reliability in the face of PVT variations. However, it should be noted that in a comparative analysis with Sudhakar's and Wang's designs, the suggested circuit experiences a delay increase of 1.1 and 1.57 times, respectively. The suggested single-trit TMUL is of the potential to integrate in larger computational circuits because it outperforms the existing design by offering improvements of at least 6.86% in power consumption and 16.67% in energy consumption, when compared to existing designs, respectively.

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Availability of Data and Materials No data associated.

Declarations

Conflict of interest None.

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