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REGULAR PAPER

An Efficient, Variation Tolerant CNTFET Ternary Content Addressable Memory a PVT Variation Resilient Design

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Abstract
Now-a-days, carbon nanotube field effect transistors (CNTFETs) are most auspicious and substitute to conventional complementary metal oxide semiconductor FETs (CMOSFETs). This because that CNTFETs have various advantages such as reduced OFF current capacity, large stability, reduced power and large ballistic transport property over the CMOSFETs. Hence, in this paper, the ternary content addressable memory (TCAM) cell is proposed using the CNTFET technology to analyze the various performances such as delay, power dissipation and power delay product (PDP), respectively. The proposed TCAM cell is developed in HSPICE simulator at 32 nm technology node using CNTFET SPICE model. The simulations shows that CNTFET TCAM cell improved the overall performance by 55.07% than the conventional CMOS based TCAM cell. The impact of process, voltage, and temperature (PVT) variations on performance of the presented TCAM cell is also investigated. It is shown that the presented TCAM cell exhibits the least amount of performance variance for PVT variations.

Keywords CNTFET · Ternary · CAM · VLSI and Nanoelectronics

1 Introduction

Due to shrinking the MOSFETs, the issues such as current leakages, increasing the power dissipation and short channel issues are become major factors [1–3]. In accordance with ITRS, the extensive research is required to design the various innovative devices and schematics that achieves the technology development in many ways [4]. To beat the issues related with the existing conventional CMOSFETs, the alternative technologies such as nanowire transistor [5, 6], FinFETs [7], tunnel FET [8], single electron transistors (SETs) [9] and CNTFETs [10–14], respectively can be utilized. Out of them, CNTFET technology outperforms the conventional MOS transistors in terms of reduced leakage current, reduced interconnect complexity reduced power consumption, high operating frequencies and avoids the short channel issues [10]. Hence, utilizing the CNTFET technology to design the various VLSI circuits is optimistic way.

When developing arrays of memory structures, the 1-bit memory is the basic building unit that represents the array. The CNTFET is a contender FET that provides large ballistic property and consumes reduced power creating it appropriate to utilize in higher performance applications. This is because of higher speed and power effective memory designs are required [15]. Moreover, CNTFET device occupies reduced area compared to the conventional CMOSFETs [10]. The multiple threshold designs (i.e., utilizing the FETs with the multiple threshold voltages) creates the CNTFET devices more attractive because of its improved performance. In CNTFETs, the threshold voltages are varied reciprocally with respect to CNT diameter which depends on CNT chirality vectors [13].

In this work, the content addressable memory (CAM) cell is designed. The CAM cell grants the access depending on data stored instead of using a physical address location. This memory cell stores data and compares it in parallel. The two main varieties of CAM are ternary CAM (TCAM) and binary CAM (BCAM), respectively. The TCAM cell provides higher information density, enhanced pattern matching, potential power savings, increased fault tolerance and so on over the BCAM cell. TCAM offers more pattern matching flexibility with usage of don't care, whereas BCAM does precise data matching. Because of this, TCAM is well-suited

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for the implementation of many network applications that including packet categorization and packet forwarding [16]. To achieve the targeted quick lookup functionality in bigger routing tables, higher performance network routers particularly require a large number of fast TCAM cells [17]. Thus, developing a small and speedy TCAM structure remains a top concern. This can be achieved by designing the TCAM cell using the CNTFET technology. Hence, in this work, the TCAM cells are developed using the CNTFETs. The CNTFET TCAM cell is designed using industry standard Synopsys based HSPICE tool. To design the CNTFET TCAM, the Stanford university CNTFET SPICE model is used. The delay, power and PDP are analysed, and compared with existing CMOSFETs. Moreover, PVT effect on performance of proposed TCAM cell is also investigated and compared with the existing CMOSFET technology.

The rest of work is arranged as follow: The literature survey on the TCAM cells is discussed in Sect. 2. The discussion on CNTFET and its characteristics are presented in Sect. 3. In Sect. 4, the proposed TCAM cell, its operation, performance and PVT variation impact are described. The conclusions of the work are presented in Sect. 5.

The main contributions of the study are fourfold:

- The TCAM Cells are developed using CNTFET technology.
- The numerical equations are presented to evaluate CNT chiral vectors, bandgap, diameters and threshold voltages.
- The HSPICE simulation tool is used to design proposed TCAM cell.
- The performance of TCAM cell is compared to the traditional TCAM cells. Moreover, the PVT variation effect on the proposed TCAM cell is investigated.

2 Literature Review on TCAM Cells

Pagiamtzis et al. [16] studied a range of CAM cell topologies and circuits, drawing attention to the enormous potential of CAMs in both these contexts. The designs of binary CAM (BCAM) and TCAM cells with MOSFETs at 180nm technology is presented in [18]. The author's compared the performance of both BCAM and TCAM cells in terms of power and speed, respectively. It is noticed that the TCAM provides lower power and large speed than BCAM. In [19], the conventional CAM cell and TCAM cell are designed. It is observed that the TCAM has low power and provides higher speed for search operation. However, the TCAM cell occupies large area compared to traditional CAM. The 4-bit CAM cell using CNTFET is proposed in [20]. The proposed 4-bit CAM cell increased the speed in 4 times higher over the existing CMOS CAM cell. The TCAM and 3-CAM cells utilizing the ambipolar CNTFETs are presented in [21]. It is observed that the 3-CAM cell improved the area up to 31% than the TCAM cell. The BCAM and TCAM cells using CNTFETs are designed in [22]. From the observations, it is noted that the TCAM improved the match delay and power consumption than the BCAM cell. In [23], the 3-CAM cell using multi-threshold devices are developed and observed the developed 3-CAM cell achieved the higher search speed and utilizes the reduced area than the conventional design. The CNTFET based TCAM cell using 16nm technology node are described in [15]. The presented TCAM cell exhibits the significant improvements in PDP for write operation, search operation and static noise margin (SNM), respectively. As per our knowledge, we found TCAM cell designs using CNTFETs and their performance but not PVT variation effect. Hence, in this work, we developed an TCAM cell using the CNTFET technology and also investigated various performance parameters for PVT variations.

3 CNTFET and Characteristics

The structure of CNTFET looks like conventional MOSFETs in which semiconductive CNTs are utilized as channel region. The threshold value (V_{CNT}) is controlled by choosing CNT chiral vectors. This is due to the fact that the V_{CNT} is determined by CNT bandgap which is determined by the alignment of the graphene layer. Typically, the alignment of the graphene layer utilized to generate the CNT that determines two numbers (n, m) that constitute the chiral vector for that specific CNT [12, 24, 25]. Additionally, according to [12, 24, 25], the CNT diameter is expressed in terms of (n, m):

$$D_{CNT} = 0.783\sqrt{n^2 + m^2 + nm} \tag{1}$$

The CNTFET structure is shown in Fig. 1. In CNTFETs, the source and drain are doped either with donor/acceptor impurities). Doping the source-terminal and drain-terminal with donor impurities is known as n-channel CNTFET, while the doping the source-terminal and drain-terminal with

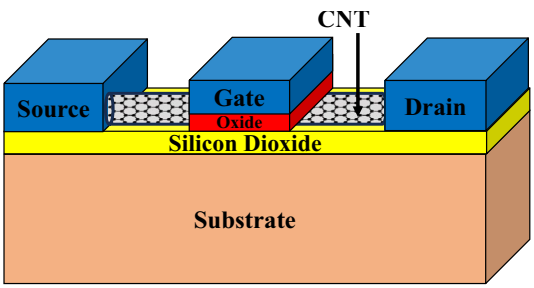

Fig. 1 Structure of CNTFET

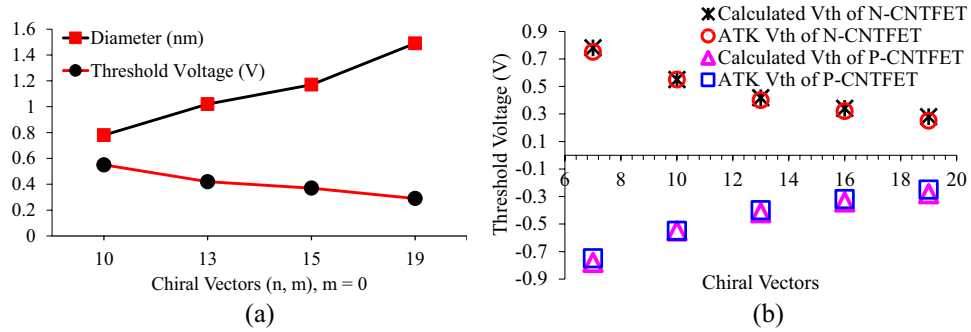

Fig. 2 **a** CNTFET Diameter and Threshold Voltage and **b** V_{th} value for various chirality vectors

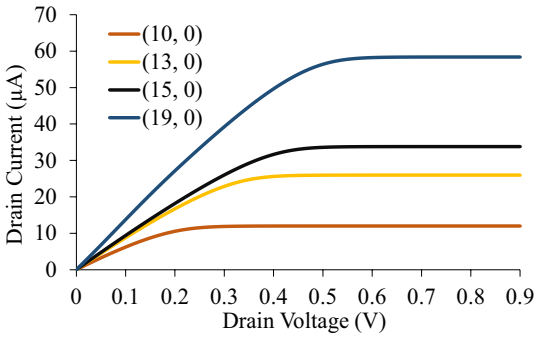

Fig. 3 CNTFET I-V curves

acceptor impurities is known as p-channel CNTFET. The undoped CNTs are organized under gate, whereas the doped CNTs are organised between gate and drain/source in this figure. This arrangement allows lower resistances which the FET is in switched ON. If the gate voltage is varied, the CNTFET is turned ON or OFF based on its V_{CNT} value. The V_{CNT} of CNTFET is expressed as [12, 24, 25].

$$V_{CNT} = \frac{aV_{pi}}{D_{CNT}} \frac{\sqrt{3}}{3e} \tag{2}$$

where V_{pi} is 3.033eV, a is C–C distance, e is charge and D_{CNT} is CNT diameter. It is obvious form Eq. (2) that the V_{CNT} of CNTFET is varies reciprocally with respect to CNT diameter. Thus, the V_{th} can be attuned to needed value by selecting proper chiral vector. The calculated values of D_{CNT} and V_{th} values of CNTFETs are illustrated in Fig. 2a. Then, the obtained calculated V_{th} values are confirmed with ATK simulations and illustrated in Fig. 2b. It is noticed calculated and ATK V_{th} values are similar. Moreover, the CNTFET I-V curves for different chiral vectors are analysed and showed in Fig. 3. It is found that CNTFET I-V curve look same as MOSFET.

4 Ternary CAM Cell Design using CNTFETs

The TCAM cell is unique that can store and retrieve ternary states (0, 1 and X). Here, X is the don't care which additional bit that acts as a wildcard entry in CAM cell. This don't care bit allows for more flexibility for the write and search functions compared to BCAM. The don't care bit is also employed for partially-matching. The schematic of proposed TCAM is illustrated in Fig. 4. Several technical and basic constraints, including power and constancy, diminish efficacy of current CMOS TCAM cells as the feature size is continuously shrunk. In order to circumvent these issues,

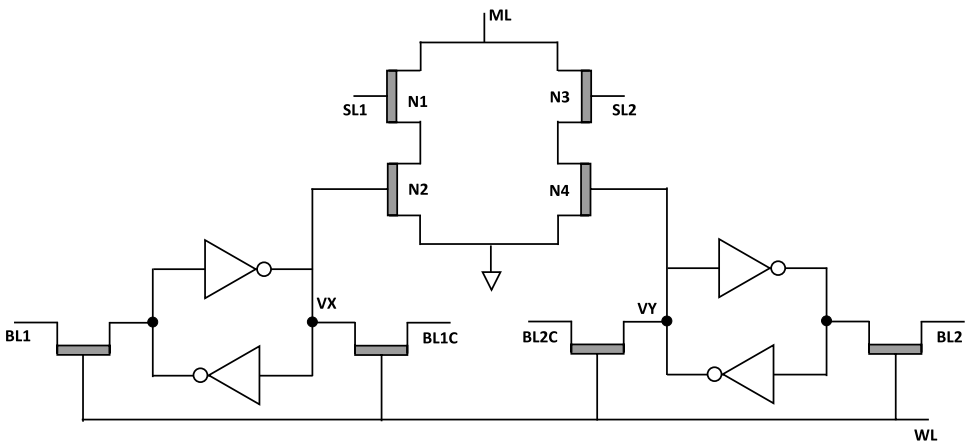

Fig. 4 Circuit diagram of the proposed TCAM cell

this study introduces the TCAM cell, which is constructed utilizing CNTFET technology. Then, the performance of the cell is evaluated by looking at its power dissipation, latency, and PDP, respectively.

The TCAM operation is also similar to existing BCAM cell. But, the difference in TCAM cell is that it consists six transistor SRAMs to store the ternary information. The four FETs M1-M4 are utilized to compare stored information along with the search key. This design gears the XNOR operation which means that when search and collected bits are same, match line is triggered. Else, it is attached to Gnd. The write and read functions are accomplished as same as SRAM. In TCAM, two SRAMs are used that stores the information 01, 10 and 11 for the logic states 0, 1 and X, respectively. Table 1 provides the logic state values of TCAM cell.

At write operation, information is positioned on bit lines (BL) and word line (WL) is enabled. Hence, it allows the writing. Moreover, the access FETs turn ON and data on BL are stored on inside nodes of cross coupled NOT gates when WL is enabled. Assume that firstly the TCAM stores the logic 1 that is $V_X = 1$ and $V_Y = 0$, the logic 0 is written by the TCAM and data on BLs are logic 0 for B_{L1} and B_{L2C} and logic 1 for B_{L2} and B_{L1C}. This happens when the WL is equal to logic 1. Then, access FETs starts conducting and resulting in BL currents. The storage node V_X is charged to logic 0 and V_Y is charged to logic 1. Figure 5 illustrates simulation response of TCAM cell for write operations.

Table 1 TCAM cell logic levels

Logic States	V_X (V)	V_Y (V)
0	0	V_{DD}
1	V_{DD}	0
X (Don't Care)	0	0

Initially, the search lines S_{L1} and S_{L2} are set to GND in search operation. Next, ML is pre-charged to high with pre-charge transistors. The next step is to apply the search data to S_{L1} and S_{L2}, respectively. The data saved at the storage node is in sync with the data that was searched for; because both pull-down pathways are turned off, match line stays at V_{DD}. One of the pull-down pathways is active, and match line is discharged to ground when stored data does not match sought data. Figure 6 shows simulations of TCAM cell for search operation. It is worth noting that proposed TCAM is simulated in HSPICE tool to obtain the responses and performances. For CNTFET based TCAM cell, The CNTFET-SPICE model discussed in [26–28] is utilized for the developing and simulating CNTFET ternary cells at 32 nm technology node with power supply 0.9V and load capacitance 0.34fF, respectively. This is typical model deliberates a realistic and schematic companionable MOSFET like CNTFET structures for SPICE simulation and comprises practical device non-idealities. The CNTFET model characteristics parameters discussed in Table 2 is used for the proposed TCAM cell simulation.

The delay, power and PDP are key metrics to decide the performance of digital circuit. Lowering the values of these metrics is needed for better performance. Figure 7 illustrates delay, power and PDP values of CNTFET TCAM at both write and search operation. Moreover, obtained delay, power and PDP values of CNTFET TCAM is compared with existing CMOS to display the efficiency of proposed study. These comparisons are shown in Fig. 7. The proposed CNTFET TCAM cell offers reduced delay, power and PDP over conventional CMOS TCAM cells. Furthermore, the obtained PDP of proposed TCAM is compared with the PDP of existing works [16, 22, 23] are placed in Table 3. The proposed TCAM cell illustrates reduced PDP over existing works.

The ternary system is very susceptible to changes in the process. As a result, simulations are run to look into how the suggested TCAM cell performs in relation to process

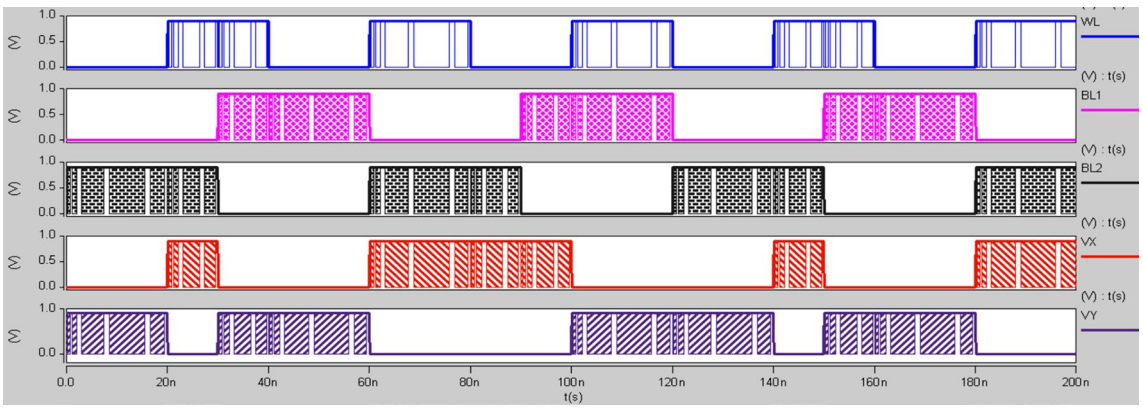

Fig. 5 Simulation response of TCAM cell for write operation

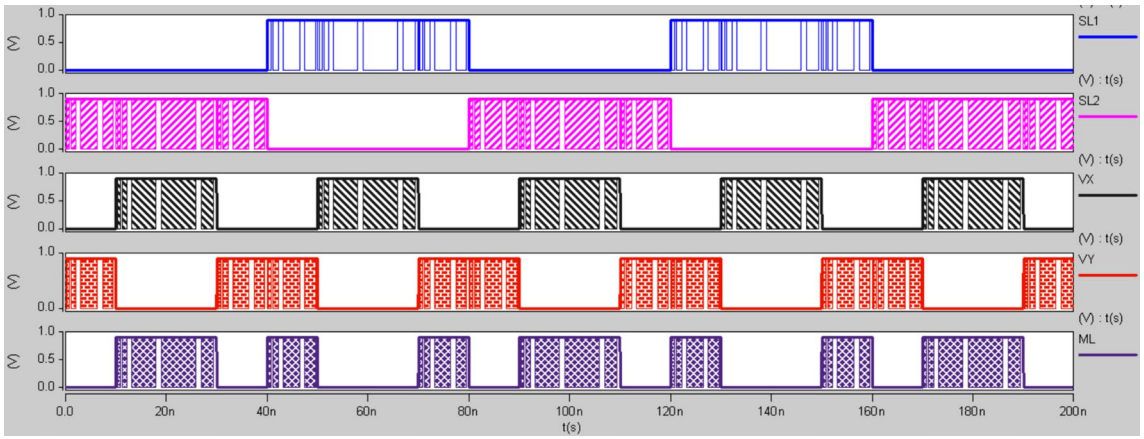

Fig. 6 Simulation response of TCAM cell for search operation

Table 2 CNTFET Model Characteristic Parameters

CNTFET Parameter	Parameter specifications	Values
L_{ch}	CNT channel	32 nm
L_{geff}	Mean free path in intrinsic CNT channel due to non-ideal elastic scattering	200 nm
L_{ss}	The length of doped CNT source-side extension terminal	32 nm
L_{dd}	The length of doped CNT drain-side extension terminal	32 nm
E_{fi}	The Fermi level of doped S/D tube	0.6 eV
K_{gate}	The dielectric constant of high-k top gate dielectric material (planer gate)	16
T_{ox}	The thickness of high-k top gate dielectric	4 nm
C_{sub}	The coupling capacitance among channel and substrate	20 pF/m

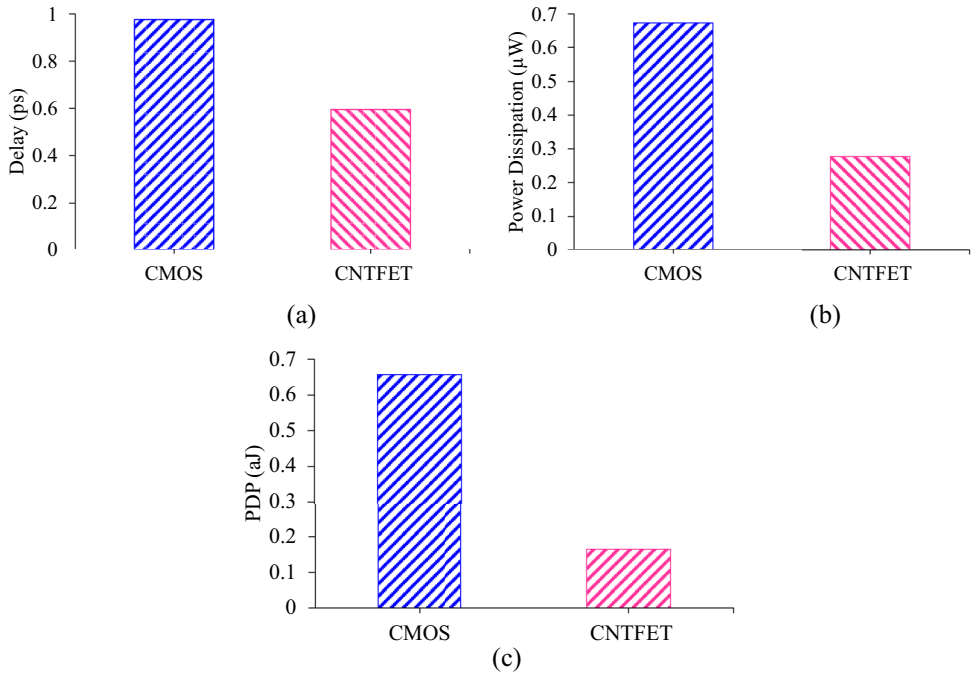

Fig. 7 Performance of TCAM cell (a) Delay, (b) Power and (c) PDP

Table 3 Comparisons of Proposed TCAM cell with Existing TCAM cells

Works	PDP values (aJ)
[22]	0.35
[23]	609.27
[16]	1.57
Proposed	0.16

variation. When evaluating performance, the impact of a transistor's gate oxide thickness is taken into account. Using the HSPICE simulator, 100 iterations per cycle are performed. Each iteration is done five times, and a significant variation is observed as a result. The suggested TCAM cell operates with minimal deviations and accuracy. Furthermore, Fig. 8 illustrate the oxide thickness impact on the latency, power, and PDP of proposed TCAM cell and the current CMOSFET TCAM cell designs.

The proposed TCAM cell's performance by changing various supply voltages are also investigated. Figure 9 compares performance (latency, power dissipation, and PDP) of TCAM cell with the CMOSFET TCAM cell for the effect of supply voltages. The presented TCAM cell shows the minimal performance variations various supply voltages. Figure 10 illustrates the influence of temperature on latency, power, and PDP, respectively. The proposed TCAM cell's latency, power dissipation, and PDP varied little with temperature. As a result, the temperature fluctuation has very little impact on performance.

The results of the CNTFET-based TCAM cell that were presented demonstrate that this technology can offer a number of benefits over the current CMOS technology, including fast speed, reduced delay, low power, and decreased PDP. These benefits emphasize signification of current research into CNTFET TCAM and its potential to help the creation of electrical devices that are more sustainable and efficient. Moreover, the presented results on CNTFET based TCAM cell shown that this study offer various advantages such as large speed, low delay, reduced power and low PDP than conventional designs. These advantages highlighting importance of continued research in CNTFET ternary cells and its potentiality for allowing advancement of high effective and sustainable electronics.

5 Conclusion

In this study, the performance of CNTFET TCAM cell is examined in terms of delay, power and PDP, respectively. The output of CNTFET TCAM reveals that TCAM cells exhibits the accurate functionality during the operation. The proposed TCAM cells are extensively simulated in industry standard Synopsys based HSPICE using CNTFET SPICE model at 32nm technology node. The attained performance such as delay, power and PDP of presented TCAM is compared to conventional CMOS TCAM cell. The presented CNTFET TCAM cell displays low delay, power and PDP

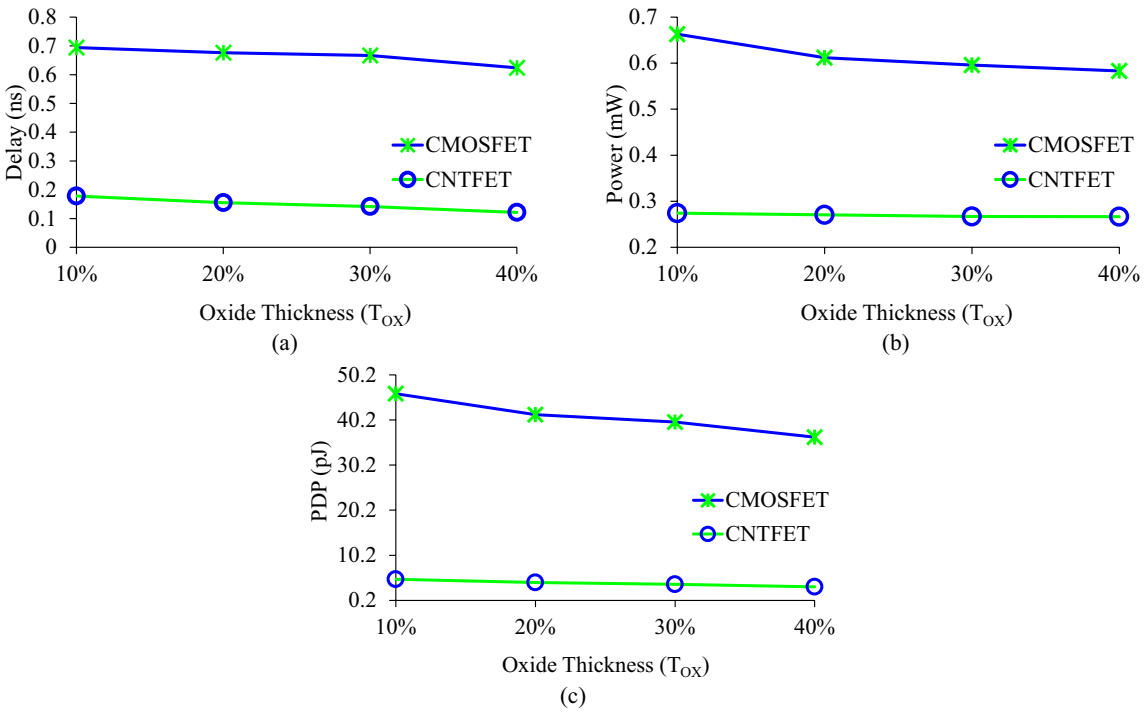

Fig. 8 Effect of T_{OX} on TCAM (a) delay, (b) power and (c) PDP

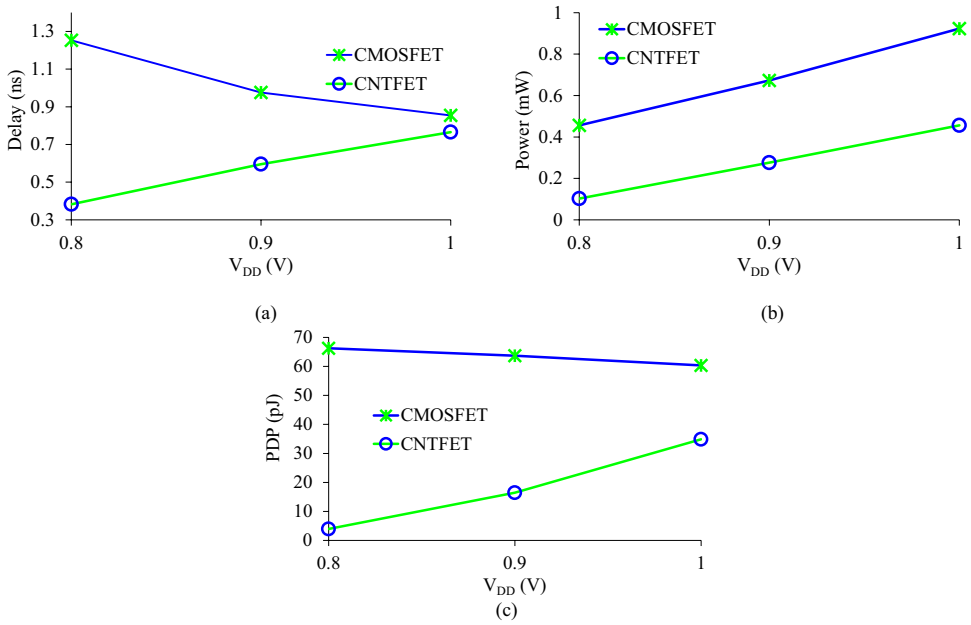

Fig. 9 Effect of V_{DD} on TCAM cell (a) delay, (b) power and (c) PDP

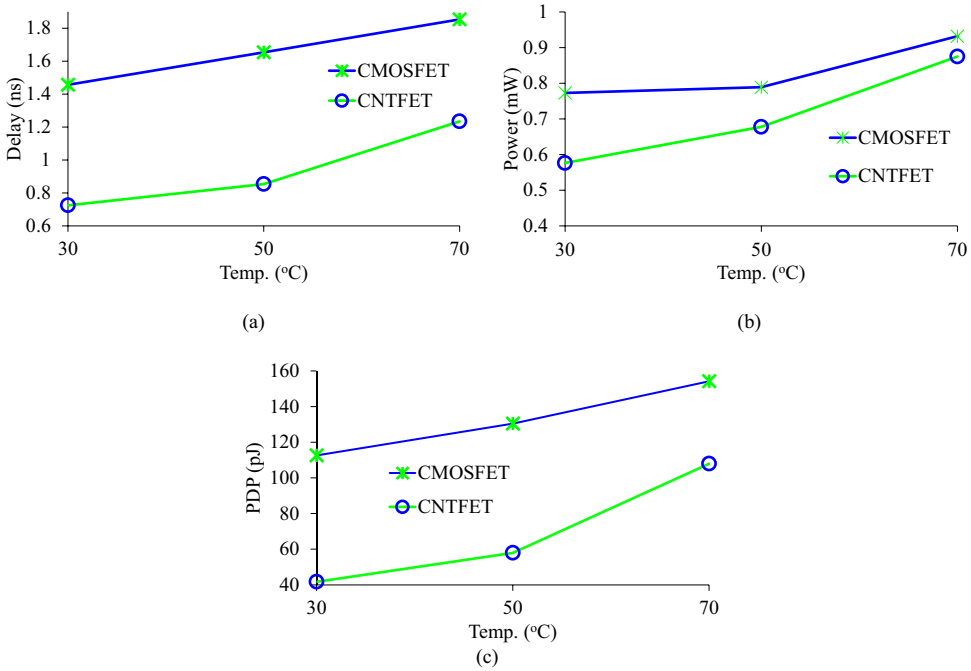

Fig. 10 Effect of temperature on TCAM cell (a) delay, (b) power and (c) PDP

than conventional CMOS TCAM. In addition, the PVT variations impact on proposed TCAM performance is analysed and noted that the least variations on performance. Because of enhancement in performance over the conventional TCAM cell, utilizing CNTFET technology to develop the memory systems offers high performance. As a future study, the different other memory cells can be designed utilizing proposed method for ternary, quaternary and quinary logic applications.

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Data availability No data has been associated.

Declarations

Conflict of interest No potential conflicts of interests.

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