



SANTHIRAM ENGINEERING COLLEGE

NANDYAL, ANDHRA PRADESH

Knowledge | Character | Progress

INSPIRE
INNOVATE
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IMPACT

WAVES

IDEAS FLOW FUTURES GROW

VOLUME 7

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ELECTRONICS & COMMUNICATION ENGINEERING

CONNECTING IDEAS
EMPOWERING PEOPLE
SHAPING TOMORROW



INNOVATE



COMMUNICATE



TRANSFORM



LEAD

*Innovate
Communicate
Transform*

A BRIGHTER
TOMORROW
THROUGH
TECHNOLOGY



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ECE Events

*New Waves
Brighter Tomorrows*

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People*



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HOD - ECE



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Department of ECE

STUDENTS
IDEAS
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ABOUT THE COLLEGE

Santhiram Engineering College (SREC) is sponsored by M/s Sri Shirdi Sai Educational Academy, Nandyal. SREC is established under the able guidance of Dr. M. Santhiramudu, Chairman in the year 2007 with a noble motto "Education for peace and progress". SREC is approved by AICTE, New Delhi; Recognized by UGC under 2(f) and 12 (B); Permanently Affiliated to JNTUA, Ananthapuramu; Certified to an ISO 9001:2015. The college is ranked as one of the Best Engineering Colleges of JNTUA, Ananthapuramu.

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LEADS
TO A BRIGHTER
TOMORROW

EDUCATION
FOR PEACE
AND PROGRESS

OUR MOTTO

EDUCATION FOR PEACE AND PROGRESS

*Knowledge
Today
A Better
Tomorrow*



Vision

To become a nucleus for pursuing technical education and pool industrial research and developmental activities with social-conscious and global standards.



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Mission

01

To provide Advance Educational Programs and prepare students to achieve success and take leading roles in their chosen fields of specialization.

02

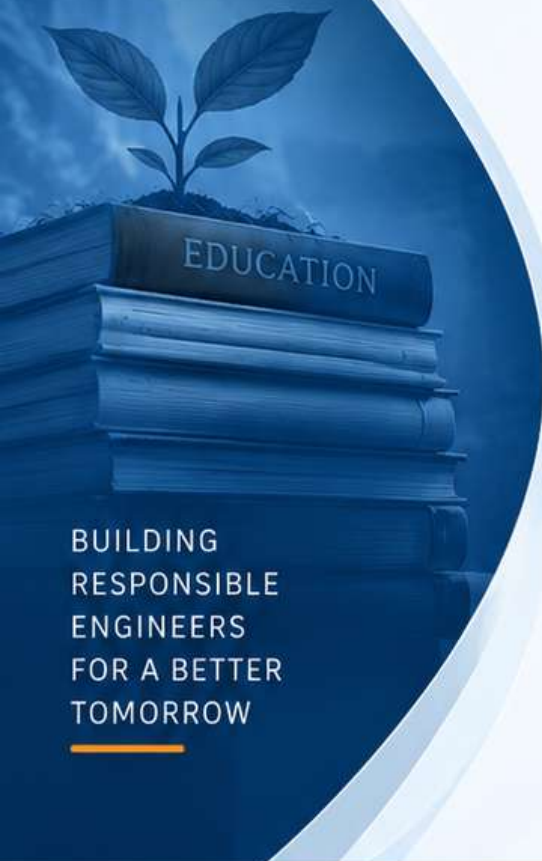
To establish postgraduate programs in the current and Advanced Technologies.

03

To establish an R&D Consultancy through developing industry institute interaction, building up exceptional infrastructure.

04

To propel every individual, realize and act for the technical development of the society.



BUILDING
RESPONSIBLE
ENGINEERS
FOR A BETTER
TOMORROW

*Together
for a Brighter Tomorrow*



ABOUT DEPARTMENT

DEPARTMENT OF ELECTRONICS AND
COMMUNICATION ENGINEERING

Anticipating the significance of the electronics and wireless communication realistic role in the society, industry and among the public, the Department of Electronics and Communication Engineering has been started carrying up its rationale since 2007 concentrating and imparting electronic & technological solutions in to the young minds of the Society. The Department was initially started with an intake of 60 seats since the opportunities are stupendous and the increase in demand for the production of engineers it is upgraded to 120 seats in 2008. Forecasting the tremendous growth & opportunities in VLSI, the Department also started a Master of Technology (M. Tech) program in VLSI System Design in the year 2011 with an intake of 12 seats. The department received an ISO 9001:2015 certification for its qualitative functioning.

The objectives of the department include: to produce quality engineers, indulge in research and promote the students to be active in entrepreneurship. The faculty has been involved in teaching and research in the diverse aspects such as Wireless Communications & Networking, Microelectronics and VLSI, Digital Image Processing and Antenna design. The department has state of the art laboratories. The faculty is entrusted to bring fine research, developmental and design experience into the classroom, ensuring that our students are being treated as professional engineers in all parts of global engineering and the scientific community.

The department extends its unwavering support for the growth of every student fulfilling their dreams. The department also extended its support to groom and nurture the qualities of teamwork, leadership, mutual understanding and co-ordination providing exposure to public and executive communication.

Technology
Empowers People

“ Signals
for a Smarter
Tomorrow



Our Vision

Emerge as a center for quality education in Electronics & Communication Engineering so as to create competent professionals.



Our Mission

M1

Offer quality programs in Electronics & Communication Engineering aimed at fulfilling the needs of society and industry.

M2

Impart skills and develop scientific temper to solve complex technological problems of current times.

M3

Nurture ethics, talent and entrepreneurship to inculcate professional development of students.

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SANTHIRAM ENGINEERING COLLEGE

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EDUCATION FOR PEACE AND PROGRESS

Learning
Today
for a Brighter
Tomorrow

Under Graduate PROGRAM OUTCOMES

- 1 Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- 2 Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- 3 Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- 4 Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- 5 Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
- 6 The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- 7 Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- 8 Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- 9 Individual and teamwork:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- 10 Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
- 11 Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- 12 Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Engineers
for a Better
Tomorrow



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Under Graduate - Program Educational Objectives (PEOs)

01

PEO1: Have in-depth knowledge in Electronics and Communication Engineering to innovate, design, and develop modern electronic systems.

02

PEO2: Sustain intellectual curiosity in professional career through life-long learning.

03

PEO3: Have strong work ethics, professional attitude, team spirit, leadership skills, and enterprising skills to serve industry and society.



Post Graduate - Program Outcomes

01

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

02

PO2: An ability to write and present a substantial technical report/document.

03

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.



Post Graduate - Program Educational Objectives (PEOs)

M. Tech. in VLSI Design Program, graduates will be able to:

01

PEO1: Identify and apply appropriate Electronic Design Automation software and electronic equipment to analyze, synthesize and evaluate to solve real-world problems in the VLSI domain to create innovative products and systems.

02

PEO2: Pursue research studies in the core or allied areas of the VLSI circuits and systems.

03

PEO3: Inculcate positive attitude, professional ethics, effective communication, and interpersonal skills to succeed in the profession exhibiting creativity and innovation through research and development both as a team member and leader.



SANTHIRAM ENGINEERING COLLEGE

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EDUCATION FOR PEACE AND PROGRESS

MESSAGES

CHAIRMAN MESSAGE



PRABODHINI of ECE Department. Exclusively meant for churning out the latent writing talent. I congratulate all the contributors for bringing out such a beautiful magazine. It bears immense potential to sharpening the students skills as part of their overall personality development. Good things remain good only because they are always scarce. It gives me immense pleasure to pen a few words as a prologue towards technical magazine PRABODHINI of ECE Department Exclusively meant for churning out the latent writing talent which bears immense potentiality of sharpening the students skills as part of their overall personality development.

Dr.M.Santhiramudu
Chairman/Founder

MD'S MESSAGE



I am pleased to learn that the department of Electronics and Communication Engineering will publish its technical magazine PRABODHINI this academic year (2022-23). This is a useful technical material and secondary skill development tool for students. I also commend the team's coordination and efforts in bringing this issue to light. I wish them all the best.

Mr. M. SivaRam
Managing Director

“

ONLY EDUCATION TO EVERY INDIVIDUAL WILL MAKE
EVERY INDIVIDUAL A CEREBRAL AND RESPONSIBLE CITIZEN

”



SANTHIRAM ENGINEERING COLLEGE

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WAVES

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*New Waves
Brighter Tomorrows*



PRINCIPAL'S MESSAGE



I am delighted to present the latest issue of WAVES, the Magazine of the Department of Electronics and Communication Engineering. A magazine is more than a compilation of articles; it is a platform that reflects the creativity, technical insight and vibrant spirit of our students and faculty. WAVES showcases their ideas, achievements and aspirations, and serves as a bridge between the present and the future.

I appreciate the earnest efforts of the Editorial Team, faculty members and students for their dedication in bringing out this issue. I am confident that WAVES will continue to inspire innovation, encourage knowledge sharing and strengthen the sense of belonging among our student community. I wish the department many more successful endeavors in the years to come.

Dr. M.V. Subramanyam
Principal



HOD'S MESSAGE



The Department of Electronics and Communication Engineering (ECE) strives to provide quality education that blends strong theoretical foundations with practical exposure. WAVES is a reflection of our department's rich academic culture, innovative mindset and the hidden talents of our students.

Our faculty members are constantly encouraging students to explore new technologies, take up challenging projects and participate in technical, cultural and social activities. I am proud of the enthusiasm and commitment shown by our students in contributing to this magazine.

I congratulate the editorial team for their sincere efforts and wish that WAVES continues to be a source of inspiration, knowledge and creativity for all readers.

Dr. Y. Mallikarjuna Rao
HOD-ECE



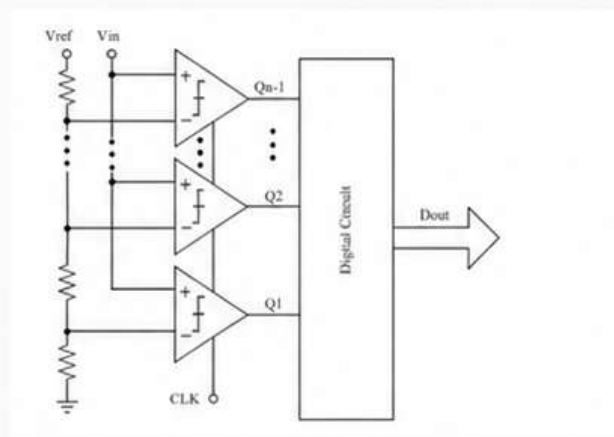
TECHNOLOGY CATCHMENT AREA

COMPARATIVE STUDY OF HIGH SPEED ADCS

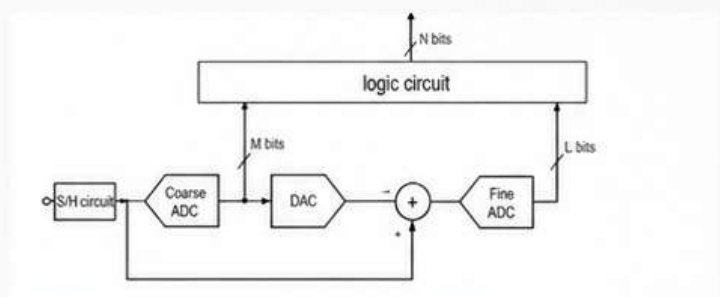
Analog-to-digital converters (ADC) are frequently employed as information technology advances. The speed performance of the analog-to-digital converter is frequently the performance bottleneck of the entire system in products like radar, ultra wideband communication system, high-performance digital oscilloscope, and others, therefore the study of high-speed ADC has drawn a lot of interest. An interface circuit called an ADC transforms analogue signals into digital signals that a DSP can process. This paper will begin with a review of the fundamentals of ADC, explain how it functions generally, discuss a number of designs and operating concepts that are appropriate for high-speed ADC, and compare and contrast the benefits and drawbacks of each.

Types of high-speed ADC

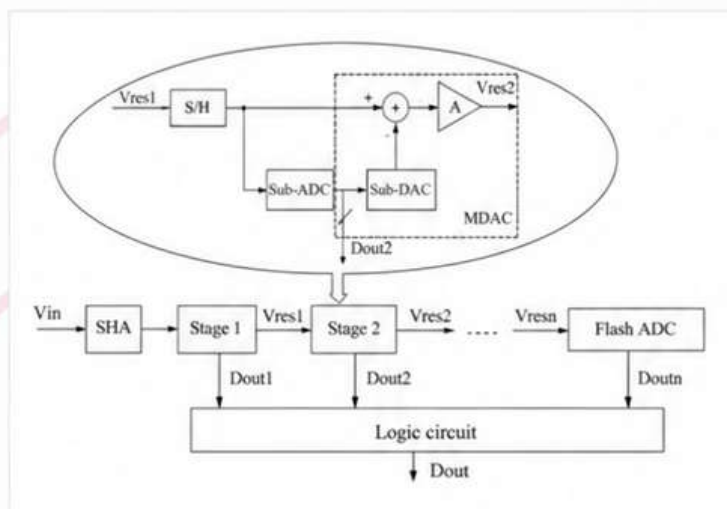
Flash adc Flash ADC can complete quantization and output at the same time in one clock cycle, without the complicated signal amplification and signal conversion process. Therefore, it has been considered as an analog-to-digital converter with the simplest structure and the highest conversion rate of single channel [4]. An n-bit full parallel ADC is shown in Figure 1. Its main body only includes a resistor string, a comparator and a digital coding circuit. The basic working process is that the input signal is connected to one input terminal of all comparators, and the other input terminal of the comparator is connected to different reference voltages, wherein the reference voltages are generated by the resistor string. At this time, the comparator obtains the digital output under the control of the clock, which is in the form of thermometer code, and needs to be converted into the commonly used binary code by the digital circuit to complete the signal conversion.



Two step adc In order to alleviate the problem that the power consumption, area and parasitic capacitance of the comparator input end of the full parallel ADC increase exponentially with the increase of the resolution, a two-step structure can be considered [5]. Its basic structure is shown in Figure 2. An n bit two-step ADC includes a sample and hold circuit, two sub ADCs (coarse quantization m bits, fine quantization L bits), a DAC circuit, a subtraction circuit and a logic circuit, where $N = M + L$. The two sub ADCs are fully parallel.



The working process of the circuit is as follows: after the input signal is sampled, it first reaches the sub ADC of the first stage, and after being quantized by it, several digital codes will be obtained. Similar to the processing of the two-step structure, this part of digital codes will enter the digital circuit for processing, and will be restored to the corresponding analog voltage signal by the sub DAC of the stage, and then the input value will be subtracted to obtain a new signal, which will be amplified by the amplifier, And then sent to the next stage circuit as its input. The next stage circuit performs the same processing as the previous stage, and then sends the signal to the next stage circuit until the quantization is completed. Since each stage circuit will output several digital codes, these digital codes will be processed and synthesized into complete digital output codes by logic circuits to realize data conversion.



Time interleaving adc Strictly speaking, the time interleaved ADC [8,9] is not an ADC with an independent architecture and cannot be paralleled with the previous ones. Time interleaving is a technology that can be applied

Folding interpolation adc Similar to the two-step ADC, the folded interpolation ADC [11,12] is also proposed to solve the problem that the number of comparators in the full parallel ADC increases exponentially with the increase of resolution. Its structural block diagram is shown in Figure 6. It can be seen from the figure that an N-bit folding interpolation ADC includes a sample and hold circuit (S/H), a folding interpolation circuit, an M-bit coarse quantization sub ADC and an L-bit fine quantization sub ADC, where $N = L + M$. In terms of structure, folded interpolation ADC is very similar to two-step ADC. Both of them generate high-order digital quantization code and low-order digital quantization code through two sub ADCs.

Folding interpolation adc Similar to the two-step ADC, the folded interpolation ADC [11,12] is also proposed to solve the problem that the number of comparators in the full parallel ADC increases exponentially with the increase of resolution. It can be seen from the figure that an N-bit folding interpolation ADC includes a sample and hold circuit (S/H), a folding interpolation circuit, an M-bit coarse quantization sub ADC and an L-bit fine quantization sub ADC, where $N = L + M$. In terms of structure, folded interpolation ADC is very similar to two-step ADC. Both of them generate high-order digital quantization code and low-order digital quantization code through two sub ADCs. The difference is that the fine quantization module in the folding interpolation ADC first performs folding preprocessing on the analog input signal, and then sends the folded signal to the fine quantization sub ADC.

Dr.G.Sowmya,
Associate Professor

Place and Route The final stage of the construction of a large design is called place and route. This is the process when all the different components of the chip is placed on its locations and connected to each other. Since a design can easily consist of thousands of connection points it would be tedious and time consuming to do the connections manually. The designer might also want to try various alternatives in placing the components, output buffers, memory structures, amplifiers, etc. The place and route tool that will be described later in this manual is named Envisia Silicon Ensemble. It is a very potent program that can place and route a very large design while respecting some design constraints (restrictions on delay and size) at the same time.

Ms.N.Jyothsna
Assistant Professor

High Speed sCMOS Camera

Digital cinema is a promising application that utilizes high-speed optical networks to transfer super high definition (SHD) images. The networks are primarily used for distributing digital cinema contents in packet data form, and are also used to support new services such as the live streaming of musicals and sport games to movie theaters.

While current transfer services offer high-definition (HD) quality video, live-streaming applications will soon shift to providing cinema quality 8K content to both business and movie theaters users.

The extra- high-quality 8K format enables a realistic telepresence, and will be combined with special tools such as video editing systems to realize effective remote collaboration for business workspaces. This paper introduces successive research on SHD image transmission and its application, especially in digital cinema and associated application fields.

Four years before the digital cinema industry standardized the DCI specification, in 2001, the worlds first video JPEG decoder system was developed that could display SHD images (38402048 pixel spatial resolution) with 24-frames/s time resolution. This decoder was designed to realize IP transmission of extra-high-quality videos, while fully utilizing the full bandwidth of emerging commercial communica-

In 2002, the second prototype SHD image decoder was developed that exploits a highly parallel processing unit of JPEG2000 de-compressors.

The decoder receives the IP streams of compressed video contents transmitted by a video server over a 1-GbE network, and decodes them using the standard JPEG2000 decoding algorithm in real time. The decoder was combined with a special 38402048 pixel projector using a dedicated digital video interface for the decoder. This architecture allows the decoded videos to be transferred and shown in completely digital form.

This system triggered detailed discussions on the digital cinema video format for DCI. The question was whether a higher image quality than HDTV was required to replace movie films. In order to solve the question, an experiment was conducted by the Entertainment Technology Center (ETC) of the University of Southern California (USC) involving 100 digital cinema engineers; it compared the image quality of conventional films, highdefinition television (HDTV), and SHD images with 8-million-pixel resolution.

The results of this experiment yielded the consensus that the horizontal resolution of around 4000 pixels was required to replace films, and JPEG2000 was suitable for the compression of digital cinema data. Stimulated by the experiment, DCI accelerated the standardization of digital cinema, specified the movie format of 40962160 pixels, and simply called it 8K. DCI finalized version 1.0 in 2005 and version 1.2 in 2008.

Currently, further standardization activities are in progress at the Society of Motion Picture and Television Engineer (SMPTE). To explore the application range of 8K video beyond digital cinema, we developed a JPEG2000-based 8K real time streaming codec system. This codec can compress/ decom- press 8K videos: the total bit rate exceeds 12 Gb/s (4 : 2 : 2, 60 frames/s), and the resulting 5001000-Mb/s compressed streams are transferred as IP packets.

8K Format

8K is a new resolution standard designed for digital cinema and computer graphics. It has following advantages:

1. Higher image definition quality.
2. More detailed picture.
3. Better fast-action.
4. Larger projection surface visibility.

8K format was named because it has 4000 pixels horizontal resolution approximately. Meanwhile, standard 1080p and 720p resolutions were named because of its vertical resolution. The new standard renders more than four times higher image definition than 1080p resolutions for example.

This format can't have the change in horizontal resolution, so changes in aspect are made through the vertical resolution. For example 40962304 is a frame size with aspect 16:9 and 40963072 - 4:3. The digital video resolutions examples:

Pixel Densities of 8K.

Full Aperture 8K 7680 * 4320 12,746,752 pixels Academy 8K 3656 x 2664 9,739,584 pixels Digital Cinema 8K 7680 x 4320 7,020,544 pixels Digital Cinema Aperture 8K 7680 x 4320 8,631,360 pixels

- a) 1920×1080 pixels, referred to as 2K.
- b) 4096×2160 pixels, referred to as 4K.
- c) 7680×4320 pixels, referred as to as 8k.

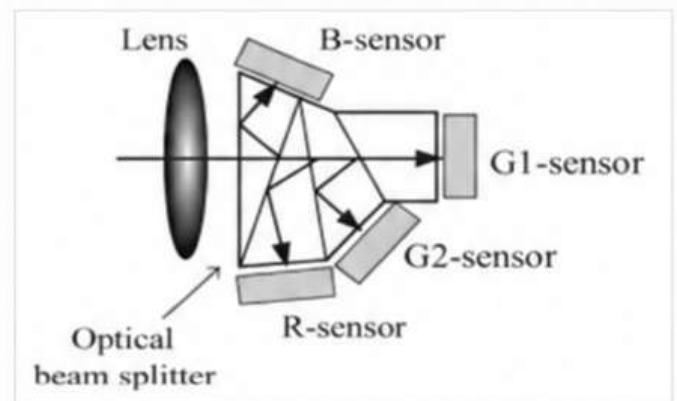
Structure of the Color Separation Prism

- Incident light is separated into four color and divided in to
- Two green, one red, and one blue (GGRB).
- Three-sensor imaging system (RGB) used in commercial and broadcast video cameras.
- Prism for the four-sensor system can be made as small as the conventional RGB prism.

Image resolution: a) 2048*1080 pixels, referred to as 2K; b) 7680*4320 pixels, referred to as 8K. The 2K format provides resolution almost equivalent to current high-definition television, while the 8K format, which has four times the resolution, provides digital images with quality as good as the conventional 35-mm film.

2. Image color reproduction and frame rate: The image quantization depth is 12 b for each XYZ color. The frame rate is the same 60 frames/s as is conventionally used for film. For the 2K format, however, a 48-frames/s mode is specified to allow for other display styles, such as the 3-D display.

3. Image compression method: JEGP2000 produces a high-quality image without the block distortion that occurs with JPEG or MPEG compression. An additional feature is that 2K resolution data can easily be extracted from 8K-resolution data. The maximum bit rate is specified as 250 Mb/s, which corresponds to about 200300 GB for a 2-h movie.



Decryption key distribution: The encryption key, which is also used for decrypting the data, is encrypted by the RSA cryptosystem of the theater exhibition equipment with license period information. It is called Key Delivery Message (KDM).

Padmavathi
20X51A0467

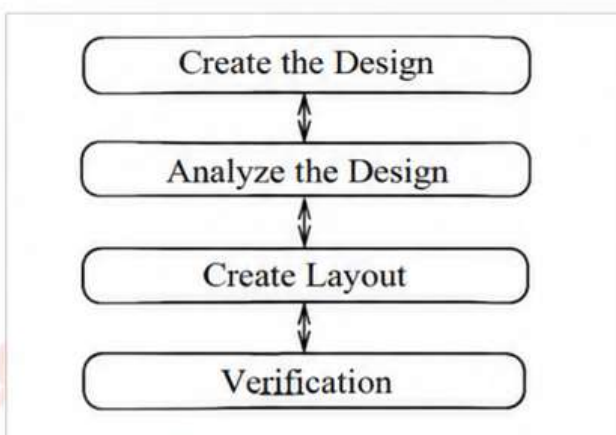
The Design Flow

The step Create the Design consists of drawing schematic views of all cells and blocks. The schematic view contains transistor symbols, and maybe other components such as resistors and capacitances, and wires connecting them. From the schematic view the symbol view is created (almost automatically) so that the cell can be used on a higher level in the hierarchy. The step Analyze the design includes functional verification (simulation) of the design on a schematic level.

The third step, Create Layout, is done in a Layout Editor. Here the final semiconductor layers are represented by different colours. All the cells and blocks used have the size they will have on the final chip. The last step is Verification of the design. The layout is examined for violations against the geometric or electrical rules, and to verify the function of the physical implementation.

Schematic and Symbol tools

To create the schematic the tool Virtuoso Schematic Composer is used. This editors an interactive system for building schematics by instantiating some basic components (transistors, capacitances, etc.) and to connect them to each other. The values (properties) of the components can be edited to suit the specifications. text and comments can also be included. The editor will also create symbols of the cells so that they can be used in other parts of the construction



Simulation

The simulation tool is started directly from the schematic editor and all the necessary netlists describing the design will be created. A simulation is usually performed in a test bench, which is also a schematic, with the actual design included as an instance. The test bench also includes signal sources and power supply. By using parameters for the properties of the components used it is possible to quickly analyze the design for a wide range of variables. The simulator is run from within Affirma Analog Circuit Design Environment which is a tool that handles the interface between the user and the simulator. The current version of Cadence used at the department (4.45) uses the Affirma Spectre Circuit Simulator. The simulator offers a wide range of analyses (DC, frequency sweep, transient, noise, etc.) and the results can be presented graphically and be saved. The results (voltage levels, currents, noise, etc.) can be fed into a calculator which can present various parameters of the analyzed circuit - delay time, rise time, slew rate, phase margin, and many other interesting properties. It is also possible to set up algebraic expressions of in or output signal which can be plotted as a function of some other variable.

Layout Tool

The Virtuoso Layout Editor is used for drawing the layout. A layout consists of geometrical figures in different colours. From the size and colour of this figures it is later possible to generate the final mask layers which is used in the fabrication of the design. It is possible to include other cells by instantiating their layout views. To verify that the layout fulfills all electrical and geometric rules a Design Rule Check (DRC) program is used. (ert to a netlist) the layout so it can be simulated.

Cadence Tools

This is a short list of tools in the Cadence suite. This isn't everything, but enough to point you to the right spot in the (openbook) documentation system.

VLSI tools (chip design, simulation, and layout)

icms - command to start an IC design desktop. This tool starts all the others listed below.

Composer - schematic capture

Analog Artist - Analog/Mixed Signal simulation framework and GUI. It is similar, but far more powerful, to PSpice Probe.

cdsSPICE - analog SPICE simulator.

Spectre - analog simulator, not based on the original Berkeley SPICE. It is still a Newton-Raphson engine, however. It does behavioral models as well as standard MOSFET, BJT, and others. I use it in preference to cdsSPICE, Berkeley SPICE, or PSpice.

Virtuoso - layout editor

DFII, Design Framework II - Database system that Cadence uses for all IC tools. Basically, all designs can be hierarchical have several views. Views can be schematics, layouts, behavioral descriptions, etc.

VHDL (hardware description language) tools:

hdlldesk - GUI desktop for HDL tools. This calls Leapfrog, cv, and ev if you want it to.

Leapfrog - simulator

cv - compiler

ev - elaborator (VHDL term for linker)

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hdlldesk - GUI desktop for HDL tools. This calls Leapfrog, cv, and ev if you want it to.

Leapfrog - simulator

cv - compiler

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Cadence User Interface

In Cadence the user interface is graphic and based on windows, forms, and menus.

The main windows of DFW are:

□ Command Interpreter Window (CIW) is controlling the environment. Other

tools can be started from here and it also serves a log window for many applications.

□ Library Manager gives a view of the design libraries and the different constructions that exists therein.

□ Design Window (DW) shows the current design. It is possible to have several DW opened at the same time with different, or the same, tools.

□ Text Window (TW) show text. It can be a log or report that was asked for, or an editor.

The menus in Cadence are mostly pull-downs, i.e. the menu will appear when the title are clicked with the left button on the mouse. There are also pop-up menus that appear in the background of the design window on a middle button press.

The forms are used for entering some specific information that is needed by the function called, the size of a transistor for instance

The SKILL Programming Language

When a command is performed, from a form or a menu, the system is executing

functions written in the SKILL language. SKILL is developed by Cadence and is based on Lisp. The Cadence tools are using SKILL for internal communication

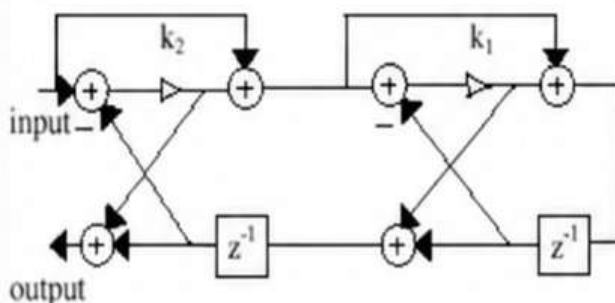
and for the tool-design communication.

SKILL is also accessible for the designers. Commands can be written in the CIW window or placed in command files for execution. it can be used for simple tasks like executing a command or building more complex functions to perform various tasks

ADAPTIVE BLIND NOISE SUPPRESSION IN SOME SPEECH PROCESSING APPLICATIONS

In many applications of speech processing the noise reveals some specific features. Although the noise could be quite broadband, there are a limited number of dominant frequencies, which carry the most of its energy. This fact implies the usage of narrow-band notch filters that must be adaptive in order to track the changes in noise characteristics. In present contribution, a method and a system for noise suppression are developed. The method uses adaptive notch filters based on second-order Gray-Markel lattice structure. The main advantages of the proposed system are that it has very low computational complexity, is stable in the process of adaptation, and has a short time of adaptation.

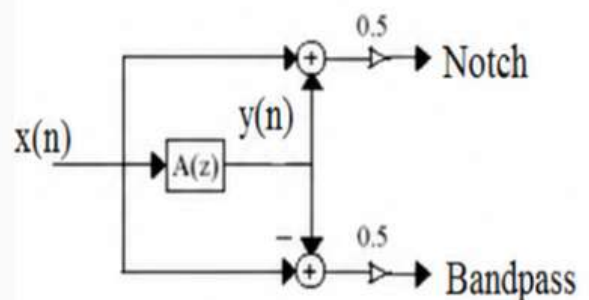
The classical systems for noise suppression rely on the usage of adaptive linear filtering and the application of digital filters with finite impulse response (FIR). The strong points of this approach are the simple analysis of the linear systems in the process of adaptation and the guaranteed stability of FIR structures. It is worth mentioning the existence of relatively simple and well investigated adaptive algorithms for such kind of systems as least mean squares (LMS) and recursive least squares (RLS) algorithms.



The classical systems for noise suppression rely on the usage of adaptive linear filtering and the application of digital filters with finite impulse response (FIR). The strong points of this approach are the simple analysis of the linear systems in the process of adaptation and the guaranteed stability of FIR structures. It is worth mentioning the existence of relatively simple and well investigated adaptive algorithms for such kind of systems as least mean squares (LMS) and recursive least squares (RLS) algorithms.

USED APPROACH FOR NOISE SUPPRESSION:

Adaptive Noise Suppression scheme has been widely adopted where the realization is based upon the Second Order Gray-Markel lattice structure, which in turn uses a Second order Notch Section. The merits for using such realization was because firstly, it could adapt to the variations in the noise characteristics very quickly with utmost ease and Secondly, it prevented any distortions in the speech signal by the application of Narrowband sections. The Following circuit below is the second order Gray-Markel lattice circuit showing the ABNS scheme.

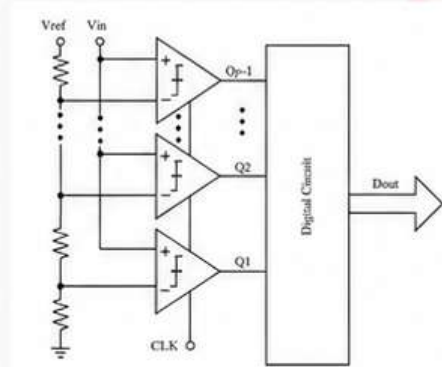


Use of Gamma Filter in place of Adaptive Notch Filter.

2. Use of Operational Amplifier(OP-AMP) In Notch Circuit.

Use Of Gamma Filter:- Gamma Filter is a new class of Adaptive IIR Filter that combines the attractive properties of Finite Impulse Response (FIR) filters with some of the power of Infinite Impulse Response (IIR) filters. Preliminary results indicate that the adaptive gamma filter is more efficient than adaline in terms of minimum mean square error. The gamma filter, a particular instance of the generalized feedforward filter, is analyzed in detail. The gamma filter borrows desirable features from both IIR and FIR systems -Stability of Gamma Filters Due to the restricted nature of the feedback loops it is easily verified that stability of gamma filter is guaranteed when $0 < \mu < 2$. In FIR and gamma filter structures, the number of adaptive parameters and the filter order are coupled (both K). Thus, when $\mu = 1$, the number of weights equals the memory depth. Very often this coupling leads to over-fitting of the data set (using parameters to model the noise). Hence, the parameter μ provides a means to decouple the memory order and depth. C. Features of Gamma Filter

1. A new class of Adaptive IIR Filter which combines the features of both FIR Filter as well as IIR filter
2. The gamma filter, a particular instance of the generalized feedforward filter, has trivial stability, easy adaptation and yet the decoupling between the region of support of the impulse response and the filter order.



Kth order filter	FIR	GAMMA	IIR
STABILITY	always stable	trivial stability $0 < \mu < 2$	non-trivial stability
MEMORY DEPTH vs. ORDER	coupled K	decoupled K/μ	decoupled
COMPLEXITY of ADAPTATION	$O(K)$	$O(K)$	$O(K^2)$

Advantages of Gamma Filter over Adaptive Notch Filter:-

- The following table highlights the major advantage of using the gamma filter:
- From the above table, we see that the Complexity of adaptation of Gamma Filter is $O(K)$, which means it is linear and hence less complex.
- We also find the complexity of FIR filter to be same as that of the Gamma filter but Gamma filter is meritorious because it can adapt quickly to the variations in the characteristics of noise which FIR filter cannot.

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Small
Thoughts
Big
Changes

INSPIRATIONAL QUOTES

THINK
LEARN
GROW



“

“Mental energy is wasted
in caste disputes and village factions.”

SRI. MOKSHA GUNDAM VISVESVARAYA

”



DISCIPLINE
DEVELOPS
NATIONS



“

“Many new technologies come with
a promise to change the world,
but the world refuses to cooperate.”

HENRY PETROSKI

”



INNOVATION
NEEDS
PERSISTENCE



“

“Take up an idea, devote yourself,
struggle in patience,
and the sun will rise.”

SWAMI VIVEKANANDA

”



ARISE
AWAKE
ACHIEVE

*Let these words guide us
towards a brighter tomorrow...*



KNOWLEDGE
CHARACTER
SUCCESS

*Be the
Change...*

CAPTURE
LEARN
SHARE
GROW

DEPARTMENT GALLERY



*Memories
that
Inspire...*

ECE EVENTS



*Students
Experiences
Success*



EXPLORE



INNOVATE



COLLABORATE



ACHIEVE