Prabhodhini

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Academic Year 2023-24

ELECTRONICS &COMMUNICATION ENGINEERING

Lorem Ipsum

SANTHIRAM ENGINEERING COLLEGE-NANDYAL

ELECTRONICS & COMMUNICATION ENGINEERING

INSIDE THIS ISSUE

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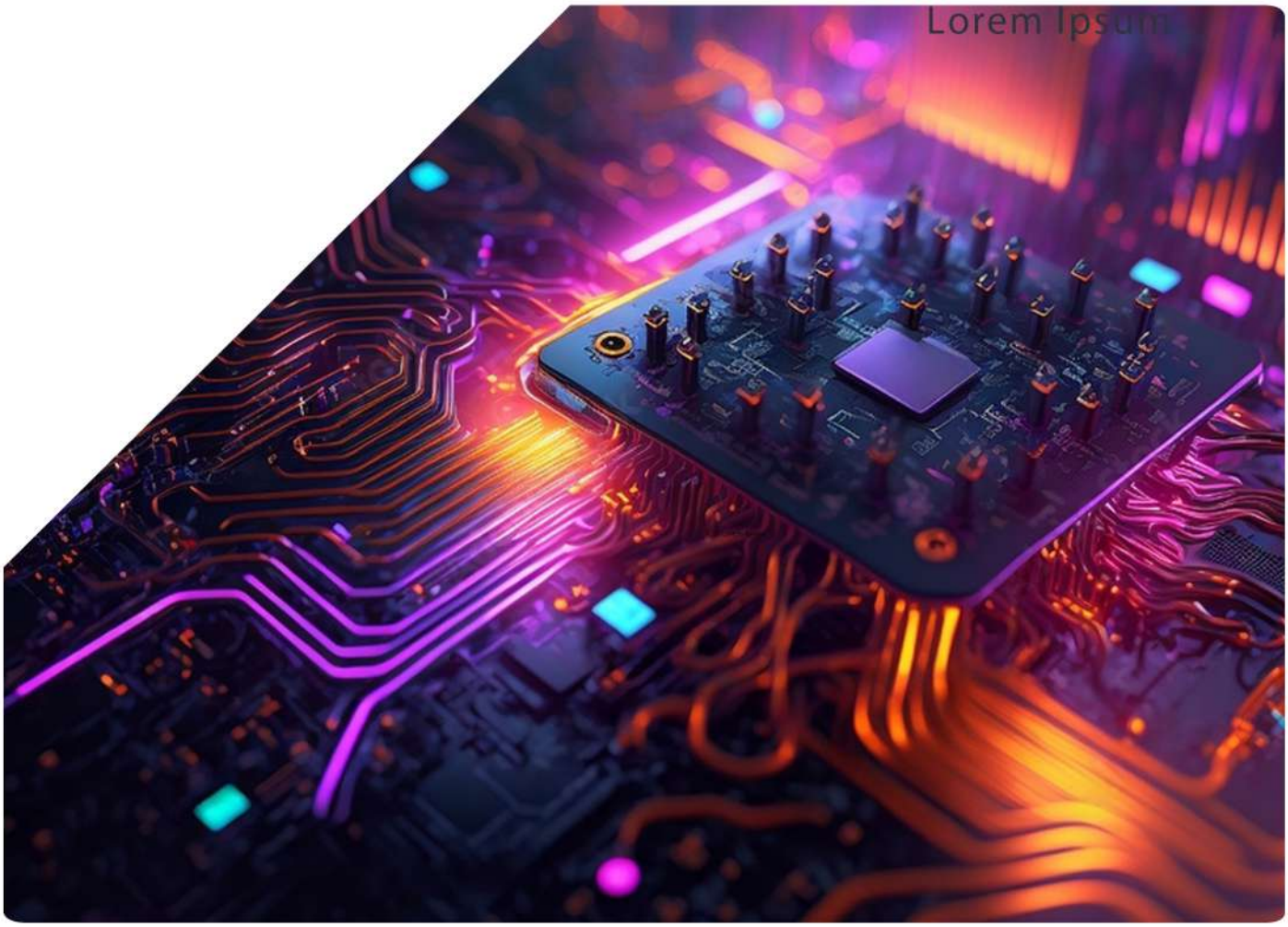


EDITORIAL BOARD

ABOUT THE COLLEGE

Santhiram Engineering College (SREC) is sponsored by M/s Sri Shirdi Sai Educational Academy, Nandyal. SREC is established under the able guidance of Dr. M. Santhiramudu, Chairman in the year 2007 with a noble motto “Education for peace and progress”. SREC is approved by AICTE, New Delhi: Recognized by UGC under 2(f) and 12 (B): Permanently Affiliated to JNTUA, Anathapuramu: Certified to anISO 9001:2015. The college is ranked as one of the Best Engineering Colleges of JNTUA. Ananthapuramu.

OUR MOTTO

EDUCATION FOR PEACE AND PROGRESS

Vision

To become a nucleus for pursuing technical education and pool industrial research and developmental activities with social-conscious and global standards.

Mission

To provide Advance Educational Programs and prepare students to achieve success and take leading roles in their chosen fields of specialization

To establish postgraduate programs in the current and Advanced Technologies

To establish an R&D Consultancy through developing industry institute interaction, building up exceptional infrastructure

To propel every individual,realize and act for the technical development of the society

ABOUT DEPARTMENT

Anticipating the significance of the electronics and wireless communication realistic role in the society, industry and among the public, the Department of Electronics and Communication Engineering has been started carrying up its rationale since 2007 concentrating and imparting electronic & technological solutions in to the young minds of the Society. The Department was initially started with an intake of 60 seats since the opportunities are stupendous and the increase in demand for the production of engineers it is upgraded to 120 seats in 2008.Forecasting the tremendous growth & opportunities in VLSI, the Department also started a Master of Technology(M. Tech) program in VLSI System Design in the year 2011 with an intake of 12 seats. The department received an ISO 9001:2015 certification for its qualitative functioning.The department received accreditation from the NBA in 2023.

The objectives of the department include: to produce quality engineers, indulge in research and promote the students to be active in entrepreneurship. The faculty has been involved in teaching and research in the diverse aspects such as Wireless Communications & Networking, Microelectronics and VLSI, Digital Image Processing and Antenna design. The department has state of the art laboratories. The faculty is entrusted to bring fine research, developmental and design experience into the classroom, ensuring that our students are being treated as professional engineers in all parts of global engineering and the scientific community.

The department extends its unwavering support for the growth of every student fulfilling their dreams. The department also extended its support to groom and nurture the qualities of teamwork, leadership, mutual understanding and co-ordination providing exposure to public and executive communication.

VISION

Emerge as a center for quality education in Electronics & Communication Engineering so as to create competent professionals.

MISSION

M1: Offer quality programs in Electronics & Communication Engineering aimed at fulfilling the needs of society and industry.

M2: Impart skills and develop scientific temper to solve complex technological problems of current times.

M3: Nurture ethics, talent and entrepreneurship to inculcate professional development of students.

Under graduate Program Outcomes

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. Individual and teamwork: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Under Graduate - Program Educational Objectives (PEOs)

1. PEO1: Have in-depth knowledge in Electronics and Communication Engineering to innovate, design, and develop modern electronic systems.
2. PEO2: Sustain intellectual curiosity in professional career through life-long learning.
3. PEO3: Have strong work ethics, professional attitude, team spirit, leadership skills, and enterprising skills to serve industry and society.

Post Graduate -Program Outcomes:-

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.
PO2: An ability to write and present a substantial technical report/document.
PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

Post Graduate -Program Educational Objectives (PEOs) :-

M. Tech. in VLSI Design Program, graduates will be able to:
1. PEO1: Identify and apply appropriate Electronic Design Automation software and electronic equipment to analyze, synthesize and evaluate to solve real-world problems in the VLSI domain to create innovative products and systems.
2. PEO2: Purse research studies in the core or allied areas of the VLSI circuits and systems.
3. PEO3: Inculcate positive attitude, professional ethics, effective communication, and interpersonal skills to succeed in the profession exhibiting creativity and innovation through research and development both as a team member and leader.

MESSAGES

CHAIRMAN MESSAGE

PRABODHINI of ECE Department. Exclusively meant for churning out the latent writing talent. I congratulate all the contributors for bringing out such a beautiful magazine. It bears immense potential to sharpening the students skills as part of their overall personality development. Good things remain good only because they are always scarce. It gives me immense pleasure to pen a few words as prologue towards technical magazine PRABODHINI of ECE Department Exclusively meant for churning out the latent writing talent which bears immense potentiality of sharpening the students skills as part of their overall personality development.

Dr.M.Santhiramudu
Chairman/Founder

MD'S MESSAGE

I am pleased to learn that the department of Electronics and Communication Engineering will publish its technical magazine PRABODHINI this academic year (2023-24). This is a useful technical material and secondary skill development tool for students. I also commend the team's coordination and efforts in bringing this issue to light. I wish them all the best.

Mr. M. SivaRam
Managing Director

" ONLY EDUCATION TO EVERY INDIVIDUAL WILL MAKE EVERY INDIVIDUAL A CEREBRAL AND RESPONSIBLE CIITIZEN "

PRINCIPAL'S MESSAGE

I am very much pleased to know that the Electronics and Communication Engineering Department has emanated out with magazine PRABODHINI. Efforts like publication of the magazine are extremely valuable on academic campuses in enhancing, developing and honing the editorial skills amongst the literary-minded students, in addition to playing the role of a mirror to the past and the possible future that holds great importance for the students. With the ever-changing priorities of the generations of the student communities that pass by the institute, such efforts can be sustained only through the commitment and dedication of the Students and Faculty members. I extend my warm patronage to all those who have contributed their best to achieve success.

Dr. M.V.Subramanyam
Principal

HOD'S MESSAGE

The Department of Electronics & Communication Engineering (ECE) has consistently maintained an exemplary academic record. The greatest asset of the department is its highly motivated and learned faculty. The available diversity of expertise of the faculty with the support of the other staff prepares the students to work in global multicultural environment. The graduates of the Electronics & Communication Stream have been selected by some of the world's leading corporations & as well as by most of the leading Indian counter parts. We hope that we will continue to deliver our best to serve the society and mankind. It is also expected that our students will continue to pass-on the skills which they have developed during their stay at this department to whole of the world for better society.

Dr.Y.Mallikarjuna Rao
HOD-ECE

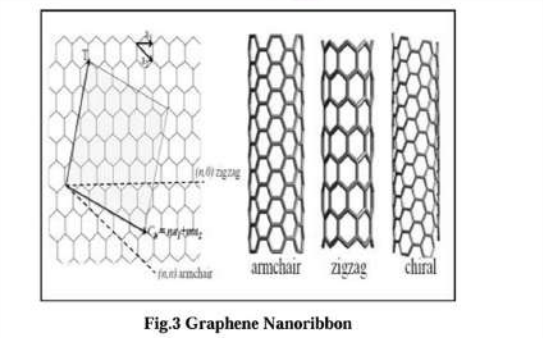


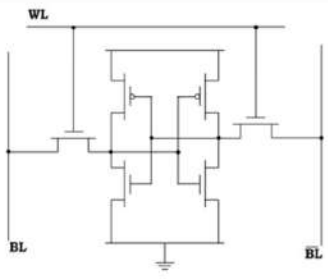
Fig.3 Graphene Nanoribbon

Graphene Nanoribbon is also called as nano-graphite ribbons, are strips of graphene with ultra-thin width (<50nm). Graphene ribbons were introduced as a theoretical model by Mitsutaka Fujita and co-authors to examine the edge and nanoscale size effect in grapheme. Careful patterning of graphene laterally confined in ribbon like structure gives rise to Graphene Nanoribbons (GNRs),

They are of two types- armchair and zigzag. In Zigzag, each segment is of opposite angle to the previous. In armchair type, each pair of segments is a 120/-120 degree rotation of the prior pair. Zigzag edges provide the edge localized state with non-bonding molecular orbitals near the Fermi energy. They are expected to have large changes in optical and elecStronic properties from quantization.

SRAM CELL

SRAM stands Static Random Access Memory. It finds application in CPU Cache, Personal Computers,
workstations, routers, hard disk buffers and router buffers. The advantage of SRAM is that it does not require periodic refreshment unlike DRAM. It is also volatile i.e. the data is lost once the power is turned off. The construction of a 6T SRAM cell consists of 2 PMOS and 4 NMOS transistors.



Mr.N.Srennivasarao,,
Asst.Professor,

Edge Detection Algorithms Uusing DeepLearning

An edge in an image is a significant local change in the image intensity. As the name suggests, edge detection is the process of detecting the edges in an image. The example below depicts an edge detection of a starfish's image.

Before reading about the HED, a question that would have popped up is, Why do we want a Deep learning algorithm for such a simple task of edge detection? The answer is that Canny edge detection focuses mainly on local changes and not on the semantics of the image i.e it focuses less on the image's content. Hence we get less accurate edges.

Deep Learning Approach for Edge Detection

A technique called Holistically Nested Edge Detection, or HED is a learning-based end-to-end edge detection system that uses a trimmed VGG-like convolutional neural network for an image-to-image prediction task. HED generates the side outputs in the neural network. All the side outputs are fused to make the final output. Let us understand the algorithm in a more detailed manner.

The VGGNet architecture, but alter it as follows:

(a) In each level, we link our side output layer to the final convolutional layer, which is conv1 2, conv2 2, conv3 3, conv4 3, and conv5 3.

(b) We remove all of the completely connected layers and the fifth pooling layer from the final stage of VGGNet. Additionally, the outputs are combined for bi-linear interpolation via in-network deconvolutional layers.

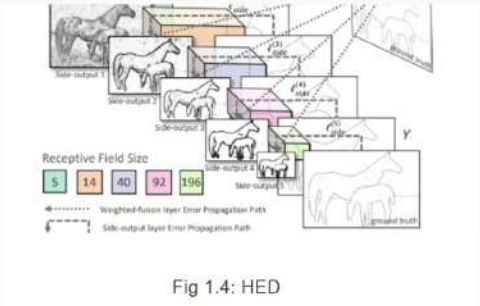


Fig 1.4: HED

ing and testing phase of the HED is covered at the end o

.The article's final portion, which involves a lot of math, discusses the HED's training and testing phase. In order to gain a better knowledge of the model design, I would advise you to take a quick look at it.

HED: Phase of Training and Testing

Let's now discuss the HED training and testing process. This is a math-heavy portion, as I indicated at the beginning of the article, so take this optional learning into consideration. I still strongly advise reading this to fully understand how HED operates.

Phase of Training

The network has M side-output layers, and W is the collection of all common network layer parameters. Every side-output layer has a classifier attached to it, where the matching weights are denoted as w = (w(1), . . . , w(m)))

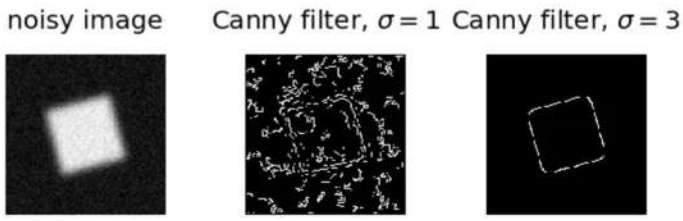
Evaluation Metrics

Now, we have understood different edge detection algorithms- Traditional and Deep Learning methods. But how do we evaluate the performance of edge detection algorithms or compare different edge detection algorithms?

This brings us to another interesting topic in edge detection – Evaluation Metrics. We will discuss different evaluation metrics for edge detection now.

Mean Squared Error

MSE represents the power of distorting noise that affects the quality of representation.



Ms.B.Alekyahimabindu
asst.Prof

UAV Networks

Unmanned Aerial Vehicles (UAVs) or drones (as they are commonly reffered to) are complex aerial wireless sensing and actuation platforms. The use of UAVs, especially quadrotors, has permeated to all aspects of human life. UAVs may effectively be used as a spatial tool in examining urban areas, including buildings, infrastructure, ecosystem features and processes, natural areas, and environmental health. Challenges, such as -- bad weather conditions, limited or absence of network connectivity, limited visual range, spread of the search zone, absence of GPS signal and other similar problems, are complex and detrimental to the use of UAVs, especially UAV swarms, in search and tracking tasks. Intelligent and dynamic automation of UAVs over networks allows for robust coordination among UAVs in a UAV network and enables solutions such as flying to specific search zones or locations, autonomously choosing appropriate UAV combinations to sense and track provided mission objectives (objectives may be tracking a plume of smoke, tracking radioactive leaks, tracking humans, and others). Intelligent automation in UAVs enables for a highly coordinated network of UAVs or UAV swarms, which can enable schemes for compensating against environmental effects to optimize tracking and minimizing the time and energy required to complete a mission. The minimization of time and energy can be addressed through optimizing the processing and analysis of data gathered from the individual drones/UAVs. The processing may be performed collaboratively within the swarm, or offloaded to a remote server. Since, there is a severe bandwidth restriction in aerial scenarios, especially if the UAV network is decentralized with no dependencies to ground-based infrastructure, there is a need for strategies to enable complex control of UAVs over networks, reducing UAV data load on the networks, deciding when and how to offload, selecting appropriate offload loactions, and many others.

In our works, we take various approaches to address the following:

A futuristic replacement for UAV Networks
Optimizing Network and UAV parameters through the use of AI/ML
Optimizing Offloading in UAV Networks
Enhancing Agricultural Practices through UAV Networks
Enabling Networked Control and Scalability of UAVs
Enhancing TArget Tracking Efficiency in UAV Networks
Virtualizing UAVs for Efficienct Resource Reuse and Re-

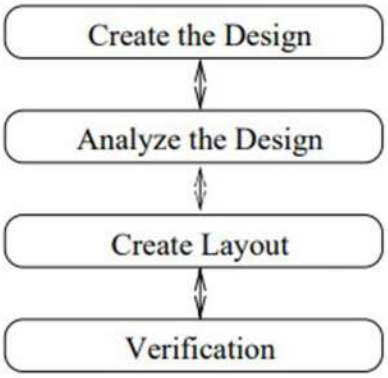
The Design Flow

The step Create the Design consists of drawing schematic views of all cells and blocks. The schematic view contains transitor symbols, and maybe other compo□nents such as resistors and capacitances, and wires connecting them. From the schematic view the symbol view is created (almost automatically) so that the cell can be used on a higher level in the hierarchy.The step Analyze the design includes functional verification (simulation) of the design on a schematic level.

The third step, Create Layout, is done in a Layout Editor. Here the final semiconductor layers are represented by different colours. All the cells and blocks used have the size they will have on the final chip. The last step is Verification of the design. The layout is examined for violations against the geometric or electrical rules, and to verify the function of the physical implementation.

Schematic and Symbol tools

To create the schematic the tool Virtuoso Schematic Composer is used. This editors an interactive system for building schematics by instanciating some basic com□ponents (transistors, capacitances, etc.) and to connect them to each other. Thevalues (properties) of the components can be edited to suit the specifications. text and comments can also be included.The editor will also create symbols of the cells so that they can be used in other parts of the construction



Simulation

The simulation tool is started directly from the schematic editor and all the nec essary netlists describing the design will be created. A simulation is usually per formed in a test bench, which is also a schematic, with the actual design included as an instance. The test bench also includes signal sources and power supply. By using parameters for the properties of the components used it is possible to quickly analyze the design for a vide range of variables. The simulator is run from within Affirma Analog Circuit Design Environmentwhich is a tool that handles the interface between the user and the simulator. The current version of Cadence used at the department (4.45) uses the Affirma Spectre Circuit Simulator. The simulator offers a wide range of analyses (DC, frequency sweep, transient, noise, etc.) and the results can be presented graphically and be saved. The results (voltage levels, currents, noise, etc.) can be fed into a calculator which can present various parameters of the analyzed circuit - delay time, rise time, slew rate, phase margin, and many other interesting properties. It is also possible to set up algebraic expressions of in or output signal which can be plotted as a function of some other variable.

Layout Tool

The Virtuoso Layout Editor is used for drawing the layout. A layout consists of geometrical figures in different colours. From the size and colour of this figures it is later possible to generate the final mask layers which is used in the fabrication of the design. It is possible to include other cells by instanciating their layout views. To verify that the layout fulfills all electrical and geometric rules a Design Rule Check (DRC) program is used.ert to a netlist) the layout so it can be simulated.

Place and Route The final stage of the construction of a large design is called place and route. This is the process when all the differnt components of the chip is placed on its locations and connected to each other. Since a design can easily consist of thousands of connection points it would be tedious and time consuming to do the connections manually. The designer might also want to try various alternatives in placing the components, output buffers, memory structures, amplifiers, etc. The place and route tool that will be described later in this manual is named Envisia Silicon Ensemble. It is a very potent program that that can place and route a very large design while respecting some design constraints (restrictions on delay and size) at the same time.

Ms.N.Jyothsna
Assistant Professor

High Speed sCMOS Camera

Digital cinema is a promising application that utilizes high-speed optical networks to transfer super high definition (SHD) images. The networks are primarily used for distributing digital cinema contents in packet data form, and are also used to support new services such as the live streaming of musicals and sport games to movie theaters.

While current transfer services offer high-definition (HD) quality video, live-streaming applications will soon shift to providing cinema quality 8K content to both business and movie theaters users.

The extra- high-quality 8K format enables a realistic telepresence, and will be combined with special tools such as video editing systems to realize effective remote collaboration for business workspaces. This paper introduces successive research on SHD image transmission and its application, especially in digital cinema and associated application fields.

Four years before the digital cinema industry standardized the DCI specification, in 2001, the worlds first video JPEG decoder system was developed that could display SHD images (38402048 pixel spatial resolution) with 24-frames/s time resolution. This decoder was designed to realize IP transmission of extra-high-quality videos, while fully utilizing the full bandwidth of emerging commercial communica-

In 2002, the second prototype SHD image decoder was developed that exploits a highly parallel processing unit of JPEG2000 de-compressors.

The decoder receives the IP streams of compressed video contents transmitted by a video server over a 1-GbE network, and decodes them using the standard JPEG2000 decoding algorithm in real time. The decoder was combined with a special 38402048 pixel projector using a dedicated digital video interface for the decoder. This architecture allows the decoded videos to be transferred and shown in completely digital form.

This system triggered detailed discussions on the digital cinema video format for DCI. The question was whether a higher image quality than HDTV was required to replace movie films. In order to solve the question, an experiment was conducted by the Entertainment Technology Center (ETC) of the University of Southern California (USC) involving 100 digital cinema engineers; it compared the image quality of conventional films, highdefinition television (HDTV), and SHD images with 8-million-pixel resolution.

The results of this experiment yielded the consensus that the horizontal resolution of around 4000 pixels was required to replace films, and JPEG2000 was suitable for the compression of digital cinema data. Stimulated by the experiment, DCI accelerated the standardization of digital cinema, specified the movie format of 40962160 pixels, and simply called it 8K. DCI finalized version 1.0 in 2005 and version 1.2 in 2008.

Currently, further standardization activities are in progress at the Society of Motion Picture and Television Engineer (SMPTE). To explore the application range of 8K video beyond digital cinema, we developed a JPEG2000-based 8K real time streaming codec system. This codec can compress/ decom- press 8K videos: the total bit rate exceeds 12 Gb/s (4 : 2 : 2, 60 frames/s), and the resulting 5001000-Mb/s compressed streams are transferred as IP packets.

8K Format

8K is a new resolution standard designed for digital cinema and computer graphics. It has following advantages:

1. Higher image definition quality.

2. More detailed picture.

3. Better fast-action.

4. Larger projection surface visibility.

8K format was named because it has 4000 pixels horizontal resolution approximately. Meanwhile, standard 1080p and 720p resolutions were named because of its vertical resolution. The new standard renders more than four times higher image definition than 1080p resolutions for example.

This format can't have the change in horizontal resolution, so changes in aspect are made through the vertical resolution. For example 40962304 is a frame size with aspect 16:9 and 40963072 - 4:3. The digital video resolutions examples:

Pixel Densities of 8K.

Full Aperture 8K 7680 * 4320 12,746,752 pixels Academy 8K 3656 x 2664 9,739,584 pixels Digital Cinema 8K 7680 x 4320 7,020,544 pixels Digital Cinema Aperture 8K 7680 x 4320 8,631,360 pixels

a) 1920×1080 pixels, referred to as 2K.

b) 4096×2160 pixels, referred to as 4K.

c)7680×4320 pixels, referred as to as 8k.

Structure of the Color Separation Prism

• Incident light is separated into four color and divided in to• Two green, one red, and one blue (GGRB).

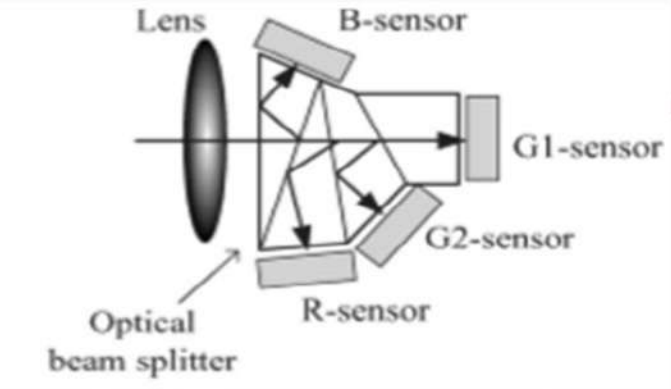
• Three-sensor imaging system (RGB) used in commercial and broadcast video cameras.

• Prism for the four-sensor system can be made as small as the conventional RGB prism.

Image resolution: a) 2048*1080 pixels, referred to as 2K; b) 7680*4320 pixels, referred to as 8K. The 2K format provides resolution almost equivalent to current high-definition television, while the 8K format, which has four times the resolution, provides digital images with quality as good as the conventional 35-mm film.

2. Image color reproduction and frame rate: The image quantization depth is 12 b for each XYZ color. The frame rate is the same 60 frames/s as is conventionally used for film. For the 2K format, however, a 48-frames/s mode is specified to allow for other display styles, such as the 3-D display.

3. Image compression method: JEGP2000 produces a high-quality image without the block distortion that occurs with JPEG or MPEG compression. An additional feature is that 2K resolution data can easily be extracted from 8K-resolution data. The max- imum bit rate is specified as 250 Mb/s, which corresponds to about 200300 GB for a 2-h movie.



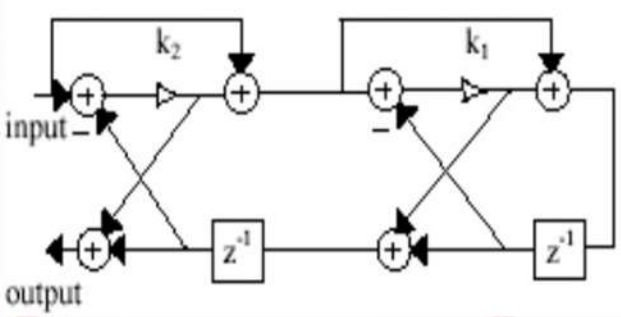
Decryption key distribution: The encryption key, which is also used for decrypting the data, is encrypted by the RSA cryptosystem of the theater exhibition equipment with license period information. It is called Key Delivery Message (KDM).

Padmavathi
20X51A0467

ADAPTIVE BLIND NOISE SUPPRESSION IN SOME SPEECH PROCESSING APPLICATIONS

In many applications of speechprocessing the noise reveals some specific features.Although the noise could be quite broadband, there are a limited number of dominant frequencies, which carry the most of its energy. This fact implies the usage of narrow-band notch filters thatmust be adaptive in order to track the changes inoise characteristics. In present contribution, a ethod and a system for noise suppression areevel-oped. The method uses adaptive notch filters based on second-order Gray-Markel latticestructure. The main advantages of the proposed system are that it has very low computational omplexity, is stable in the process of adaptation, and has a short time of adaptation.

The classical systems for noise suppression rely on the usage of adaptive linear filtering and the application of digital filters with finite impulsere onse (FIR). The strong points of this approach are the simple analysis of the linear systems in the process of adaptation and the guaranteed stability of FIR structures. It is worth mentioning the existence of relatively simple and well investigated adaptive algorithms for such kind of systems as least mean squares (LMS) and recursive least squares (RLS) algorithms



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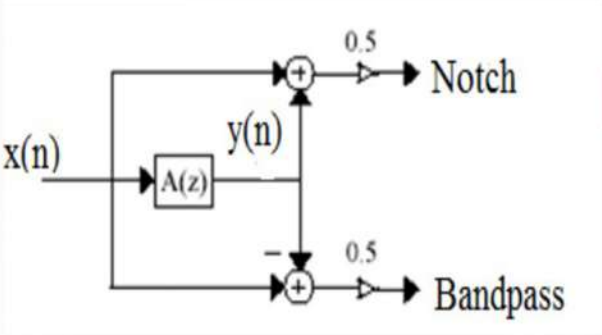
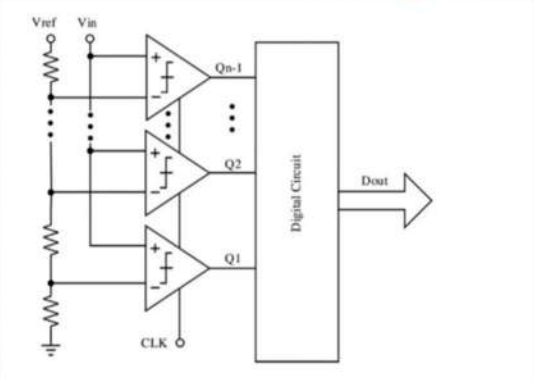
USED APPROACH FOR NOISE SUPPRESSION:
Adaptive Noise Suppression scheme has been widely adopted where the realization is based upon the Second Order Gray-Markel lattice structure, which in turn uses a Second order Notch Section. The merits for using such realization was because firstly, it could adapt to the variations in the noise characteristics very quickly with utmost ease and Secondly, it prevented any distortions in the speech signal by the application of Narrowband sections. The Following circuit below is the second order Gray-Markel lattice circuit showing the ABNS scheme.



Use of Gamma Filter inplace of Adaptive Notch Filter.
2. Use of Operational Amplifier(OP-AMP) In Notch Circuit.

Use Of Gamma Filter:- Gamma Filter is a new class of Adaptive IIR Filter that combines the attractive properties of Finite Impulse Response (FIR) filters with some of the power of Infinite Impulse Response (IIR) filters. Preliminary results indicate that the adaptive gamma filter is more efficient than adaline in terms of minimum mean square error. The gamma filter, a particular instance of the generalized feedforward filter, is analyzed in detail. The gamma filter borrows desirable features from both IIR and FIR systems -Stability of Gamma Filters Due to the restricted nature of the feedback loops it is easily verified that stability of gamma filter is guaranteed when $0 < \mu < 2$. In FIR and gamma filter structures, the number of adaptive parameters and the filter order are coupled (both K). Thus, when $\mu = 1$, the number of weights equals the memory depth. Very often this coupling leads to overfitting of the data set (using parameters to model the noise). Hence, the parameter μ provides a means to decouple the memory order and depth. C. Features of Gamma Filter 1. A new class of Adaptive IIR Filter which combines the features of both FIR Filter as well as IIR filter. 2. The gamma filter, a particular instance of the generalized feedforward filter, has trivial stability, easy adaptation and yet the decoupling between the region of support of the impulse response and the filter order.



Kth order filter	FIR	GAMMA	IIR
STABILITY	always stable	trivial stability $0 < \mu < 2$	non-trivial stability
MEMORY DEPTH vs. ORDER	coupled K	decoupled K/μ	decoupled
COMPLEXITY of ADAPTATION	O(K)	O(K)	$O(K^2)$

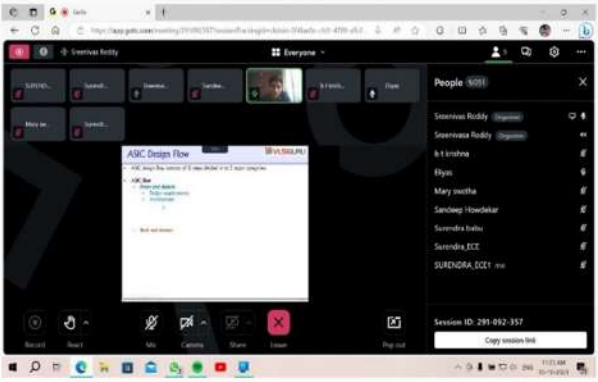
Advantages of Gamma Filter over Adaptive Notch Filter:- • The following table highlights the major advantage of using the gamma gilter: • From the above table, we see that the Complexity of adaptation of Gamma Filter is O(K),which means it is linear and hence less complex. • We also find the complexity of FIR filter to be same as that of the Gamma filter but Gamma filter is meritous because it can adapt quickly to the variations in the characteristics of noise which FIR filter cannot.

Mr.E.Yaswanth
20X51A0413

ECE EVENTS

A one-week faculty development program on "Recent Trends in VLSI Technologies and Practical Approaches towards IP Using EDA Tools" in association with JNTUA was conducted by e Department of ECE from 9-13 Oct,2023.

A webinar on "recent trends and challenges in VLSI and career opportunities was conducted by Department of ECE on 5



A one-day program on career opportunities in VLSI design and manufacturing was conducted by e Department of ECE on 12 Oct-.

INSPIRATIONAL QUOTES

MENTAL ENERGY IS WASTED IN CASTE DISPUTES AND VILLAGE FACTIONS.

SRI. MOKSHA GUNDAM VISVESVARAYA

MANY NEW TECHNOLOGIES COME WITH A PROMISE TO CHANGE THE WORLD, BUT THE WORLD REFUSES TO COOPERATE.

HENRY PETROSKI

TAKE UP AN IDEA, DEVOTE YOURSELF, STRUGGLE IN PATIENCE, AND THE SUN WILL RISE.

SWAMI VIVEKANANDA